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Note : Remove “Table of Content” before including in CP Book

EE

Each Course Plan shall be printed and made into a book with cover page

Blooms Level in all sections match with A.2, only if you plan to teach / learn at higher levels

18EE35 : Digital System Design

A. COURSE INFORMATION

1. Course Overview

Degree:	B.E	Program:	EE
Year / Semester :	3rd / 3rd	Academic Year:	2019-20
Course Title:	Digital System Design	Course Code:	18EE35
Credit / L-T-P:	3 / 4-0-0	SEE Duration:	180 Minutes
Total Contact Hours:	50	SEE Marks:	60 Marks
CIA Marks:	40	Assignment	1 / Module
Course Plan Author:	Kiranmayi M	Sign	Dt:03-08-2019
Checked By:		Sign	Dt:

2. Course Content

Module	Module Content	Teaching Hours	Module Concepts	Blooms Level
1	Definition of combinational, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3, 4 and 5 variables. Incompletely specified functions (Don't care terms). Simplifying max - term equations. Quine -McClusky minimization technique, Quine - McClusky using don't care terms, Reduced Prime Implicant tables.	10	Combinational circuits Boolean algebra	L2, L3
2	General approach, Decoders-BCD decoders, Encoders. Digital multiplexers-using multiplexers as Boolean function generators. Adders and Subtractors-Cascading full adders, Look ahead carry, Binary comparators. Design methods of building blocks of combinational logics.	10	Boolean function generators Ar-thematic circuits	L4
3	Basic Bistable element, Latches, SR latch, application of SR latch, A Switch debouncer, The gated SR latch. The gated D Latch, The Master-Slave Flip-Flops (Pulse-Triggered Flip-	10	Flip flops	L2, L4

	Flops): The master-slave SR Flip-Flops, The master-slave JK Flip-Flop. Characteristic equations, Registers, Counters-Binary Ripple Counter, Synchronous Binary counters, Counters based on Shift Registers, Design of a Synchronous counters, Design of a Synchronous Mod-6 counters using clocked JK Flip-Flops Design of a Synchronous Mod-6 counter using clocked D, T, or SR Flip Flops		Counters	
4	Introduction, Mealy and Moore models, State machine notation, synchronous sequential circuit analysis and design. Construction of state Diagrams, Counters Design.	10	State machines Sequential circuit design	L2, L4
5	Introduction, A brief history of HDL, Structure of HDL Module, Operators, Data types, Types of Descriptions (only VHDL), Simulation and synthesis, Brief comparison of VHDL and Verilog. Data-Flow Highlights of Data flow descriptions, Structure of data-flow description	10	HDL data-flow description	L2

3. Course Material

Module	Details	Available
1	Text Books	
1.1	Digital Logic Applications, John M Yarbrough, CengageLearn, 2011	In Lib
1.2	Digital Principles and Design, Donald D, McGraw Hill, 1st Edition, 2002	In Lib
2	Reference books	
2.1	Logic and computer design,Fundamentals, M. Morries Mano and Charles Kime Pearson Learning 4th , Edition, 2014	
2.2	Fundamentals of logic design, Charles H Roth, JR and Larry L. Kinney,Cengage Learning 6th Edition, 2013	
2.3	Fundamentals of Digital Circuits, A. Anand Kumar, PHI 3rd Edition, 2014	
2.4	Digital Logic Design and VHDL, A.A.Phadke, S.M.Deokar, Wiley India 1st Edition, 2009	
2.5	Digital Circuits and Design, D.P.KothariJ.S.Dhillon Pearson First Print 2015	
2.6	HDL Programming (VHDL and Verilog) Nazeih M. Botros Cengage Learning1 Edition, 2011	
2.7	Circuit Design and Simulation with VHDL Volnei A Pedroni PHI 2nd Edition	
3	Others (Web, Video, Simulation, Notes etc.)	
3.1	NPTL vedios	Available
3.2	Wikipedia	Available

3.3	Written notes	Available

4. Course Prerequisites

SNo	Course Code	Course Name	Module / Topic / Description	Sem	Remarks	Blooms Level
1	17ELN24	Basic Electronics	1. Knowledge Digital Electronics Fundamentals	2		L2

Note: If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.

B. OBE PARAMETERS

1. Course Outcomes

#	COs	Teach. Hours	Concept	Instr Method	Assessment Method	Blooms' Level
18EE35.1	Understand the SOP & POS expressions & their simplifications from truth table.	5	Combinational circuits	Lecture	Assignment Unit Test & IA	L2 Understanding
18EE35.2	Solving max terms of SOP & POS using simplification techniques like k-map, Quine -McClusky minimization & Reduced Prime Implicant tables.	8	Boolean algebra	Lecture	Assignment Unit Test & IA	L3 Apply
18EE35.3	Analyze & Design of Boolean Expressions using Decoders & Multiplexers.	7	Boolean function generators	Lecture	Assignment Unit Test & IA	L4 Analyze
18EE35.4	Analyze & Design of Adders & Subs tractors using K-map	7	Ar-thematic circuits	Lecture	Assignment Unit Test & IA	L4 Analyze
18EE35.5	Understand the logics of Flip flops & Latches using Logic diagrams &	8	Flip flops	Lecture	Assignment	L2 Understandi

	verifying with truth table.				Unit Test & IA	ng
18EE35.6	Analyze & Design of counters using clocked D,T or SR flip flops.	8	Counters	Lecture	Assignment Unit Test & IA	L4 Analyze
18EE35.7	Understand the Mealy & Moore models using their Block diagrams.	5	State machines	Lecture	Assignment Unit Test & IA	L2 Understanding
18EE35.8	Analyze & Design of Sequential circuits using State & state transition technique.	8	Sequential circuit design	Lecture	Assignment Unit Test & IA	L4 Analyze
18EE35.9	Understand the structure of HDL, operators using block diagram & compare between VHDL & Verilog.	5	HDL	Lecture & PPT	Assignment Unit Test & IA	L2 Understanding
18EE35.10	Understand the structure of Data flow description using block diagram & flowchart.	5	data-flow description	Lecture & PPT	Assignment Unit Test & IA	L2 Understanding
	Total	**66**	**-**	**-**	**-**	**-**

Note: Identify a max of 2 Concepts per Module. Write 1 CO per concept.

2. Course Applications

SNo	Application Area	CO	Level
1	Used in design of adder	CO1	L2
2	Automated Cafeteria	CO2	L3
3	To effective data exchange In communication system and to implement home alarm system	CO3	L4
4	In forming ALU for desinging CPU to GPU	CO4	L4
5	In formation of Registers	CO5	L2
6	To Set an AC timer, Flashing indicator lights of your vehicle, etc	CO6	L4
7	To designing the sequential circuits & Can be used in video controller	CO7	L2
8	To design Elevator, vending machine, etc.	CO8	L4

9	Used for chip design and automation system..	CO9	L2
10	Used in transferring data.	CO10	L2

Note: Write 1 or 2 applications per CO.

3. Articulation Matrix

(CO – PO MAPPING)

-	Course Outcomes	Program Outcomes												
#	COs	PO1	PO 2	PO 3	PO 4	PO 5	PO6	PO 7	PO 8	PO9	PO 10	PO 11	PO 12	Level
18EE35.1	Understand the SOP & POS expressions & their simplifications from truth table.	X												L2
18EE35.2	Solving max terms of SOP & POS using simplification techniques like k-map, Quine -McClusky minimization & Reduced Prime Implicant tables.	X	X											L3
18EE35.3	Analyze & Design of Boolean Expressions using Decoders & Multiplexers.	X	X	X										L4
18EE35.4	Analyze & Design of Adders & Subs tractors using K-map	X		X	X									L4
18EE35.5	Understand the logics of Flip flops & Latches using Logic diagrams & verifying with truth table.		X	X	X									L2
18EE35.6	Analyze & Design of counters using clocked D,T or SR flip flops.	X		X	X									L4
18EE35.7	Understand the Mealy & Moore models using their Block diagrams.	X												L2
18EE35.8	Analyze & Design of Sequential circuits using State & state transition technique.	X	X	X										L4
18EE35.9	Understand the structure of HDL, operators using block diagram & compare between	X		X										L2

	VHDL & Verilog.													
18EE35.10	Understand the structure of Data flow description using block diagram & flowchart.	X		X										L2

Note: Mention the mapping strength as 1, 2, or 3

4. Mapping Justification

Mapping		Justification	Mapping Level
CO	**PO**	**-**	**-**
CO1	PO1	Applying the knowledge to simplify complex circuits.	L2
CO2	PO1	Knowledge of Boolean algebra helps the students in circuit designing	L3
CO2	PO2	Analysis of circuit provide the students for better understanding of digital circuits	L4
CO3	PO1	Its sound foundation to analyze digital circuits	L4
CO3	PO2	Choose a simplified circuit for implementing a combinational circuit using an appropriate simplification method	L2
CO3	PO3	Designing of complex combinational circuits	L4
CO4	PO1	This knowledge required to design mathematical circuits	L2
CO4	PO3	Designing of complex combinational circuits	L4
CO4	PO4	Choose a simplified circuit for implementing a combinational circuit using an appropriate simplification method	L2
CO5	PO2	Having knowledge in Flip flop and latches students could develop sequential circuit	L2
CO5	PO3	Knowledge of Flip flops could be used to reduce the complexity of the sequential circuit	L2
CO5	PO4	Having the knowledge in various sequential circuit design principles students could analyze the problem and come to a conclusion on which design principle to be use	L3
CO6	PO1	Knowledge in counter design helps to find solutions for complex engineering problems in digital electronics	L4
CO6	PO3	Knowledge in counter design helps digital electronics engineers to develop solutions for complex Engineering problems	L4
CO6	PO4	Choose a simplified circuit for implementing a Sequential circuit using an appropriate Flip flop.	L2
CO7	PO1	An understanding state models helps to design automated machines.	L4
CO8	PO1	Knowledge in State Machines helps to find solutions for complex automated machines.	L2
CO8	PO2	Knowledge in State Machines helps to analyze complex automated machines	L4

CO8	PO3	Basic principles of State Machines help to design a complex automated machine.	L2
CO9	PO1	Knowledge in HDL fundamentals help the students to do electronics program and digital logic circuits.	L2
CO9	PO3	Apply the suitable algorithms to design digital logic circuits	L2
CO10	PO1	Knowledge required to know the flow of data graphically	L3
CO10	PO3	Apply the suitable algorithms in data transferring	L4

Note: Write justification for each CO-PO mapping.

5. Curricular Gap and Content

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1	Simulation Tools	Demo			
2	Practical use of number system	Assignment			
3	Practical use of flip flops	Seminar			
4	Design of circuits	Practical			
5	Application of flip flops in computers	Practical			

Note: Write Gap topics from A.4 and add others also.

6. Content Beyond Syllabus

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
5					
7					
8					
9					
10					

Note: Anything not covered above is included here.

C. COURSE ASSESSMENT

1. Course Coverage

Module #	Title	Teaching Hours	No. of question in Exam						CO	Levels
			CIA-1	CIA-2	CIA-3	Asg	Extra Asg	SEE		

1	Principles of combinational logic	13	2	-	-	1	1	2	CO1, CO2	L2, L3
2	Principles of combinational logic	14	2	-	-	1	1	2	CO3, CO4	L4, L4
3	Sequential Circuits	16	-	2	-	1	1	2	CO5, CO6	L2, L4
4	Sequential Design	13	-	2	-	1	1	2	CO7, C08	L2, L4
5	HDL & Data-Flow Descriptions	10	-	-	4	1	1	2	CO9, CO10	L2, L2
-	**Total**	**66**	**4**	**4**	**4**	**5**	**5**	**10**	**-**	**-**

Note: Distinct assignment for each student. 1 Assignment per chapter per student. 1 seminar per test per student.

2. Continuous Internal Assessment (CIA)

Evaluation	Weightage in Marks	CO	Levels
CIA Exam – 1	30	CO1, CO2, CO3, CO4	L2, L3, L4, L4
CIA Exam – 2	30	CO5, CO6, CO7, C08	L2, L4, L2, L4
CIA Exam – 3	30	CO9, CO10	L2, L2
Assignment – 1	10	CO1, CO2, CO3, CO4	L2, L3, L4, L4
Assignment – 2	10	CO5, CO6, CO7, CO8	L2, L4, L2, L4
Assignment – 3	10	CO9, CO10	L2, L2
Seminar – 1			
Seminar – 2			
Seminar – 3			
Other Activities – define – Slip test			
Final CIA Marks	**40**	**-**	**-**

Note : Blooms Level in last column shall match with A.2 above.

D1. TEACHING PLAN – 1

Module – 1

Title:	Principles of combinational logic	Appr Time:	16 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Understand the SOP & POS expressions & their simplifications from truth table.	CO1	L2
2	Solving max terms of SOP & POS using simplification techniques like	CO2	L3

	k-map, Quine -McClusky minimization & Reduced Prime Implicant tables.		
b	***Course Schedule***		–
Class No	**Module Content Covered**	**CO**	**Level**
1	Definition of combinational	C01	L2
2	canonical forms	CO1	L2
3	Generation of switching equations from truth tables,	CO1	L3
4	Karnaugh maps-3, 4 and 5 variables.	CO2	L3
5	Incompletely specified functions (Don't care terms).	CO2	L3
6	Simplifying max - term equations.	CO2	L3
7	Quine -McClusky minimization technique,	CO2	L3
8	Quine - McClusky using don't care terms,	CO2	L3
9	Reduced Prime Implicant tables.	CO2	L3
c	**Application Areas**	**CO**	**Level**
1	To express the boolean expressions	CO1	L2
2	To simplify the Switching equations	CO2	L3
d	**Review Questions**	–	–
1	Explain combinational logic Circuit with the help of block diagram	C01	L2
2	Define the following terms along with appropriate examples for better explanation a.Literal b.Minterm c.Maxterm d.Canonical SOP e.Canonical POS f.Normal SOP	C01	L2
3	What are the different ways of simplifying a Boolean expression	C01	L2
4	What are canonical forms illustrate with an example	C01	L2
5	Reduce the following function using K-Map technique and implement using Basic gates. a. $f(X,Y,Z) = \sum(0,2,4,6) + dc(7)$ b. $f(X,Y,Z) = \prod(0,3,5,6).dc(7)$ c. $f(P,Q,R,S) = \sum m(0,1,4,8,9,10) + dc(2,11)$ d. $f(A,B,C,D) = \prod M(0,2,4,10,11,14,15)$	C01	L3
6	Reduce the following function using K-Map technique and implement using only the NAND gates. a. $f(A,B,C,D) = \sum(0,2,5,7,8,10,13,15) + dc(9,11)$ b. $f(A,B,C,D) = \prod(3,4,6,11,12,14).dc(7,15)$ c. $f(A,B,C,D) = \sum(1,3,4,6,9,11) + dc(5,7)$ d. $f(A,B,C,D) = \prod(0,1,2,5,9,11).dc(7,13)$	C01	L3
7	Convert the Sum of products expression to its Canonical form a. $f(a,b,c) = (ac + ab + bc)$ b. $f(a,b,c) = a.(abc)$ c. $f(a,b,c) = (ab' + bc)$	C01	L3

8	Express the following SOP expressions into minterm list form and hence write maxterm list a. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$ b. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$	C01	L3
9	Design a logic circuit with inputs P, Q, R so that output S is high whenever P is zero or whenever Q=R=1	C01	L3
10	Design a logic circuit that has 4 inputs, the output will only be high, when the majority of the inputs are high, Use K – Map to simplify	C01	L3
11	Design a logic circuit that has 4 inputs, the output will only be high, when the majority of the inputs are high, Use K – Map to simplify	C01	L3
12	Design a logic circuit that controls the passage of a signal 'A' according to the following requirement. a.Output 'X' will equal 'A' when control inputs B and C are the same. b.'X' will remain 'HIGH' when B and C are different. Implement the circuit using suitable gates	C01	L3
13	Staircase light is controlled by two switches; one is at the top of the stair and other at the bottom of the stairs. a.Make a truth table for this system. b.Write the logic equations in the SOP form. c.Realize the circuit using basic gates. Realize the circuit using minimum number of NAND gates	C01	L3
14	Design a combinational logic circuit, which converts BCD code into Excess-3 code and draw the circuit diagram.	C01	L3
15	Distinguish between prime implicants and essential prime implicants. Determine the same of the function using K-map & hence the minimal sum expression. $f(w,x,y,z) = \sum m(0,1,4,5,9,11,13,15)$	C01	L3
16	Two motors M2 and M1 are controlled by three sensors S3, S2, S1. One motor M2 is to run any time all three sensors are on. The other motor is to run whenever sensors S2 or S1 but not both are on and S3 is off. For all sensor combinations where M1 is on, M2 is to be off except when all the three sensors are off and then both motors must remain off. Construct the truth table and write the Boolean output equation.	C01	L3
17	Express the Product of Sums equations in a maxterms list (decimal notations) form a. $f(a,b,c) = (a+b'+c)(a+b'+c)(a'+b'+c')$ b. $f(a,b,c,d) = (a+b'+c+d)(a+b'+c+d')(a'+b+c+d)(a'+b'+c+d)(a'+b+c'+d)(a'+b'+c'+d)$	C01	L3
18	Convert the Product of Sums expression to its Canonical form a. $f(a,b,c) = (a+b)(b+c)(a+c)$ b. $f(a,b,c) = a.(a+b+c)$ c. $f(a,b,c) = (b+c').(ab'+c)$	C01	L3
19	Convert the Sum of products expression to its Canonical form a. $f(a,b,c) = (ac + ab + bc)$ b. $f(a,b,c) = a.(abc)$ c. $f(a,b,c) = (ab' + bc)$	C01	L3
20	Express the following SOP expressions into minterm list form and hence write maxterm list a. $f(a,b,c,d) = (a\,b\,c + ab\,d + abcd + a\,b\,cd + abc'd)$ b. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$	C01	L3
21	Simplify using Quine McClusky tabulation algorithm $Y = f(a,b,c,d) = \sum m(2,3,4,5,13,15) + dc(8,9,10,11)$	CO2	L3

22	Simplify the logic function given below, using Quine - McClusky minimization technique. $Y(A,B,C,D) = \sum m(0,1,3,7,8,11,15)$, Realize the simplified expression using universal gates.	CO2	L3
23	Using Quine McClusky method and prime implicant reduction table, Obtain the Minimal sum expression for the function	CO2	L3
24	Obtain the minimal product of the following Boolean functions using (VEM) technique. $Y = f(a,b,c,d) = \sum m(1,5,7,10,11) + dc(2,3,6,13)$	CO2	L3
25	Simplify the following expression using Quine-McClusky technique and implement using basic gates. $f(A,B,C,D) = \sum m(1,3,4,5,6,9,11,12,13,14)$	CO2	L3
26	Minimize $f(a,b,c,d) = \pi M(0,6,7,8,9,13) + \pi d(5,15)$ using Quine – McClusky method.	CO2	L3
27		CO2	L3
28	Find all the Prime Implicants of the function $f(a,b,c,d) = \pi M(0,2,3,4,5,12,13) + \pi d(8,10)$ using Quine Mc-Cluskey method.	CO2	L3
29	For the following Boolean function use the Quine Mc-Cluskey method to obtain all the prime implicants and apply Petrick's method to find the irredundant disjunctive normal expressions and identify the minimal sums. $f(a,b,c,d) = \sum m(4,5,7,12,14,15)$	CO2	L3
30	Find a minimal sum for the following incomplete Boolean function using decimal notation Quine Mc-cluskey method. $f(a,b,c,d) = \sum m(7,9,12,13,14,15) + \sum d(4,11)$	CO2	L3
31	Write the map entered variable K – Map for the Boolean function $f(w,x,y,z) = \sum m(2,9,10,11,13,14,15)$	CO2	L3
32	Simplify using variable entered mapping (VEM) technique and implement using basic gates. $f(a,b,c,d) = A'B'C'D' + A'B'C'D + AB'C'D' + A'BC'D' + A'B'C'D' + A'B'C'D' + A'B'C'D'$	CO2	L3

e	**Experiences**	–	–
1		CO1	L2
2			
3			
4		CO3	L3
5			

Module – 2

Title:	Analysis and design of Combinational Logic	Appr Time:	10 Hrs
a	***Course Outcomes***	–	**Blooms**
–	The student should be able to:	–	**Level**
1	Analyze & Design of Boolean Expressions using Decoders & Multiplexers.	CO3	L4
2	Analyze & Design of Adders & Subs tractors using K-map	CO4	L4
b	***Course Schedule***	–	–
Class No	**Module Content Covered**	**CO**	**Level**
17	General approach	CO3	L2
18	Decoders-BCD decoders	CO3	L4
19	Encoders	CO3	L2
20	Digital multiplexers-using multiplexers as Boolean function generators.	CO3	L4
21	Adders and Subtractors-Cascading full adders	CO4	L3
22	Look ahead carry	CO4	L3
23	Binary comparators.	CO4	L4
24	Design methods of building blocks of combinational logics.	CO4	L4
c	**Application Areas**	**CO**	**Level**
1	To effective data exchange In communication system	CO3	L4
2	In forming ALU for desinging CPU to GPU	CO4	L4

d	**Review Questions**	-	-
1	Design a combinational logic circuit, which converts BCD code to Excess-3 code and draw the circuit diagram.	CO3	L4
2	Design a combinational logic circuit that will multiply two 2-bit binary values	CO3	L4
3	Design a combinational logic circuit to output the 2's complement of a 4-bit binary numbers: a) Construct the truth table. b) Simplify each output equation using K-map an write reduced equations. c) Draw the resulting logic diagram	CO3	L4
4	Design a combinational logic circuit to find 9's complement of a BCD number	CO3	L4
5	Design a combinational logic circuit to drive a common cathode seven segment display with BCD inputs	CO3	L4
6	Design a combinational logic circuit to output a 1 when an illegal BCD code occurs	CO3	L4
7	Design a combinational logic circuit to drive a common anode seven segment display with BCD inputs	CO3	L4
8	Design a Combinational Circuit that accepts two unsigned 2-bit binary no. and provides 3 outputs. Inputs: A=A1A0 and B= B1B0 Output: A=B, A>B, A<B.	CO3	L4
9	Develop the logic diagram of a 2 to 4 decoder with the following specifications: a)Active low enable input. b) Active high encoded outputs. Draw the IEEE symbol.	CO3	L3
10	Write the condensed truth table for 0,4, to 2 line priority encoder with a valid output where the highest priority is given to the highest bit position or input with highest index and obtain the minimal sum expressions for the outputs	CO3	L3
11	Describe the general working principle of decoder	CO3	L2
12	With the aid of block diagram, clearly distinguish between a decoder and encoder	CO3	L2
13	Implement a full subtractor using a decoder and NAND gates	CO4	L3
14	Design a logic circuit using a 3 to 8 logic decoder that has active low data inputs, an active HIGH enable and active low data outputs. Use such a decoder to realize the full adder circuit	CO4	L4
15	Designa 4 to 16 decoder using two 3 to 8 decoder (74LS138).	CO3	L4
16	Design a keypad interface to a digital system using ten line BCD encoder	CO3	L4
17	Implement a full adder using a decoder	CO3	L3
18	Implement 3-bit binary to gray code conversion by using IC 74139	CO3	L3
19	Design a priority encoder for a system with a 3 inputs, the middle bit with highest priority encoding to 10, the MSB with next priority encoding to 11, while the LSB with least priority encoding to 01	CO3	L4

20	Write a note on encoders.	CO3	L2
21	What are the problem associated with the basic encoder explain how can these problems be overcome by priority encoder, considering 8-bit input lines.	CO3	L2
22	Implement the multiple functions: a)$f(a,b,c,d) = \sum m(0,4,8,10,14,15)$. b) $f(a,b,c,d) = \sum m(3,7,9,13)$. Using two 3 to 8 decoders.	CO3	L4
23	Implement the following with a suitable decoder with active low enable input and active high output: a) $f(w,x,y,z) = \sum m(3,7,9)$ b)$f(a,b,c,d) = \pi d(2,4,7)$.	CO3	L4
24	Realize the following Boolean functions using 74139. a) $f(w,x) = \sum m(0,2)$ b) $f(a,b,c) = \sum m(1,3,6,7)$.	CO3	L4
26	Configure a 16 to 1 MUX using 4 to 1 MUX.	CO3	L4
27	Design 2-bit comparator using gates	CO3	
28	Design a 4-bit BCD adder circuit using IC7483, with self correcting circuit. ie, a provision has to be made in the circuit, in case if the sum of BCD number exceeds 9.	CO4	L4
29	Design and implement a 4-bit look ahead carry adder.	CO4	L4
30	Implement a 12-bit comparator using IC7485.	CO4	L3
31	Design a comparator to check if two n-bit numbers are equal. Configure these using cascaded stages of 1-bit comparators.	CO4	L4
32	Design a binary full adder using minimum number of gates.	CO4	L4
33	Explain the following terms a)Ripple carry propagation b)Propagation delayc)Look ahead carry d)Iterative design.	CO4	L2
34	Design a binary full subtractor using minimum number of gates.	CO4	L4
35	Explain 4-bit Parallel adder and subtractor.	CO4	L2
36	Explain Decimal adder.	CO4	L2
37	Explain Decimal adder.	CO4	L2
38	Implement the following Boolean function with 8:1 multiplexer $f(a,b,c,d) = \sum m(0,2,6,10,11,12,13) + \sum d(3,8,14)$	CO3	L4
39	Design a full adder using MUX. For a full adder S= $\sum m(1,2,4,7)$ C = $\sum m(3,5,6,7)$	CO4	L4
40	Implement the following function using 4:1 MUX $f(a,b,c) = \sum m(1,3,5,6)$	CO3	L4
e	**Experiences**	-	-
1			

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E1. CIA EXAM – 1

a. Model Question Paper – 1

Crs Code:	17EE35	Sem:	III	Marks:	30	Time:	75 minutes
Course:	Design and Analysis of Algorithms						

-	-	**Note: Answer any 3 questions, each carry equal marks.**	**Marks**	**CO**	**Level**
1	a	Design a logical Circuit, when Two motors M2 and M1 are controlled by three sensors S3, S2 and S1. One motor M2 is to run any when all the three sensors are ON. The other motor is to run when ever sensors S2 or S1 but not both are ON and S3 is OFF. For all sensors combinations where M1 is ON, M2 is OFF, except when all the three sensors are OFF and then both motors must remain OFF.	5	CO1	L3
	b	Reduce the following functions using K-map technique and implement using Gates. (i) f(P,Q,R,S) = Σm (0,1,4,8,9,10) (ii) f(A,B,C,D) = ΠM (0,2,4,10,11,14,15)	5	CO1	L3
	c	Express the following SOP expressions into minterm list form and hence write maxterm list a. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$ b. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$	5	CO1	L3
2	a	Find a minimal sum for the following incomplete Boolean function using Decimal Q-M method and prime implicant table reduction f(a,b,c,d) = Σm (2,3,4,5,13,15) + Σd (8,9,10,11)	8	CO2	L3
	b	For a given incomplete Boolean function find a minimal sum & minimal product using MEV technique using A, B & C as map variables F(A,B,C,D) = Σm (1,5,6,7,9,11,12,13) + Σd (0,3,4)	7	CO2	L3
3	a	Design 32:1 Multiplexer using only IC74150.	5	CO3	L4
	b	Design a combinational circuit to find 9,s complement of a BCD number, realize the circuit using suitable Logic gates.	5	CO3	L4
	c	Realize the following Boolean function P=f(w,x,y,z) =Σ(0,1,5,6,7,10,15) using (i) 16 to 1 MUX (ii) 8 to 1 MUX (iii) 4 to 1 MUX	5	CO3	L3

4	a	With a neat logic diagram, Explain Carry look ahead adder.	5	CO4	L2
	b	What is comparator? Design 2-bit comparator and implement with suitable logic gates.	5	CO4	L4
	c	Write a note on encoders.	5	CO3	L3

b. Assignment -1

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions							
Crs Code:	17EE35	Sem:	III	Marks:	5	Time:	90 – 120 minutes
Course:	Design and Analysis of Algorithms						

Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.

SNo	USN	Assignment Description	Marks	CO	Level
1	1KT17EE001	What are the different ways of simplifying a Boolean expression	5	C01	L2
2	1KT17EE002	What are canonical forms illustrate with an example	5	C01	L2
3	1KT17EE003	Reduce the following function using K-Map technique and implement using Basic gates. a. $f(X,Y,Z) = \sum(0,2,4,6) + dc(7)$ b. $f(X,Y,Z) = \prod(0,3,5,6).dc(7)$ c. $f(P,Q,R,S) = \sum m(0,1,4,8,9,10) + dc(2,11)$ d. $f(A,B,C,D) = \prod M(0,2,4,10,11,14,15)$	5	C01	L3
4	1KT17EE005	Reduce the following function using K-Map technique and implement using only the NAND gates. a. $f(A,B,C,D) = \sum(0,2,5,7,8,10,13,15) + dc(9,11)$ b. $f(A,B,C,D) = \prod(3,4,6,11,12,14).dc(7,15)$ c. $f(A,B,C,D) = \sum(1,3,4,6,9,11) + dc(5,7)$ d. $f(A,B,C,D) = \prod(0,1,2,5,9,11).dc(7,13)$	5	C01	L3
5	1KT17EE007	Convert the Sum of products expression to its Canonical form a. $f(a,b,c) = (ac + ab + bc)$ b. $f(a,b,c) = a.(abc)$ c. $f(a,b,c) = (ab' + bc)$		C01	L3
6	1KT17EE008	Express the following SOP expressions into minterm list form and hence write maxterm list a. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$ b. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$	5	C01	L3
7	1KT17EE009	Design a logic circuit that controls the passage of a signal 'A' according to the following requirement. a.Output 'X' will equal 'A' when control inputs B and C are the same. b.'X' will remain 'HIGH' when B and C are different. Implement the circuit using suitable gates	7	C01	L3
8	1KT17EE010	Staircase light is controlled by two switches; one is at the top of the stair and other at the bottom of the stairs. a.Make a truth table for this system. b.Write the logic equations in the SOP form. c.Realize the circuit using basic gates. Realize the circuit using minimum number of NAND	7	C01	L3

		gates			
9	1KT16EE003	Design a combinational logic circuit, which converts BCD code into Excess-3 code and draw the circuit diagram.	7	C01	L3
10	1KT16EE010	Distinguish between prime implicants and essential prime implicants. Determine the same of the function using K-map & hence the minimal sum expression. $f(w, x, y, z) = \sum m(0,1,4,5,9,11,13,15)$	7	C01	L3
11	1KT16EE005	Two motors M2 and M1 are controlled by three sensors S3, S2, S1. One motor M2 is to run any time all three sensors are on. The other motor is to run whenever sensors S2 or S1 but not both are on and S3 is off. For all sensor combinations where M1 is on, M2 is to be off except when all the three sensors are off and then both motors must remain off. Construct the truth table and write the Boolean output equation.	7	C01	L3
12	1KT18EE400	Simplify the following expression using Quine-McClusky technique and implement using basic gates. $f(A, B, C, D) = \sum m(1,3,4,5,6,9,11,12,13,14)$	8	CO2	L3
13	1KT18EE401	Minimize $f(a, b, c, d) = \pi M(0,6,7,8,9,13) + \pi d(5,15)$ using Quine – McClusky method.	8	CO2	L3
15	1KT17EE001	Find all the Prime Implicants of the function $f(a, b, c, d) = \pi M(0,2,3,4,5,12,13) + \pi d(8,10)$ using Quine Mc-Cluskey method.	10	CO2	L3
16	1KT17EE002	For the following Boolean function use the Quine Mc-Cluskey method to obtain all the prime implicants and apply Petrick's method to find the irredundant disjunctive normal expressions and identify the minimal sums. $f(a, b, c, d) = \sum m(4,5,7,12,14,15)$	10	CO2	L3
17	1KT17EE003	Find a minimal sum for the following incomplete Boolean function using decimal notation Quine Mc-cluskey method. $f(a, b, c, d) = \sum m(7,9,12,13,14,15) + \sum d(4,11)$	10	CO2	L3
18	1KT17EE005	Write the map entered variable K – Map for the Boolean function $f(w, x, y, z) = \sum m(2,9,10,11,13,14,15)$	8	CO2	L3
19	1KT17EE007	Simplify using variable entered mapping (VEM) technique and implement using basic gates. $f(a, b, c, d) = A'B'C'D' + A'B'C'D + AB'C'D' + A'BC'D' + A'B'C'D' + A'B'C'D' + A'B'C'D'$	8	CO2	L3
20	1KT17EE008	Design a combinational logic circuit, which converts BCD code to Excess-3 code and draw the circuit diagram.	7	CO3	L4
21	1KT17EE009	Design a combinational logic circuit that will multiply two 2-bit binary values	5	CO3	L4
22	1KT17EE010	Design a combinational logic circuit to output the 2's complement of a 4-bit binary numbers: a) Construct the truth table. b) Simplify each output equation using K-map an write reduced equations. c) Draw the resulting logic	5	CO3	L4

		diagram			
23	1KT16EE003	Design a combinational logic circuit to find 9's complement of a BCD number	5	CO3	L4
24	1KT16EE010	Design a combinational logic circuit to drive a common cathode seven segment display with BCD inputs	7	CO3	L4
25	1KT16EE005	Design a combinational logic circuit to output a 1 when an illegal BCD code occurs	5	CO3	L4
26	1KT18EE400	Design a combinational logic circuit to drive a common anode seven segment display with BCD inputs	7	CO3	L4
27	1KT18EE401	Design a Combinational Circuit that accepts two unsigned 2-bit binary no. and provides 3 outputs. Inputs: A=A1A0 and B= B1B0 Output: A=B, A>B, A<B.	7	CO3	L4
28	1KT17EE001	Develop the logic diagram of a 2 to 4 decoder with the following specifications: a)Active low enable input. b) Active high encoded outputs. Draw the IEEE symbol.	5	CO3	L3
29	1KT17EE002	Write the condensed truth table for 0,4, to 2 line priority encoder with a valid output where the highest priority is given to the highest bit position or input with highest index and obtain the minimal sum expressions for the outputs	5	CO3	L3
30	1KT17EE003	Describe the general working principle of decoder	5	CO3	L2
31	1KT17EE005	With the aid of block diagram, clearly distinguish between a decoder and encoder	5	CO3	L2
32	1KT17EE007	Implement a full subtractor using a decoder and NAND gates	5	CO4	L3
33	1KT17EE008	Design a logic circuit using a 3 to 8 logic decoder that has active low data inputs, an active HIGH enable and active low data outputs. Use such a decoder to realize the full adder circuit	5	CO4	L4
34	1KT17EE009	Designa 4 to 16 decoder using two 3 to 8 decoder (74LS138).	7	CO3	L4
35	1KT17EE010	Design a keypad interface to a digital system using ten line BCD encoder	7	CO3	L4
36	1KT16EE003	Implement a full adder using a decoder	5	CO3	L3
37	1KT16EE010	Implement 3-bit binary to gray code conversion by using IC 74139	5	CO3	L3
38	1KT16EE005	Design a priority encoder for a system with a 3 inputs, the middle bit with highest priority encoding to 10, the MSB with next priority encoding to 11, while the LSB with least priority encoding to 01	7	CO3	L4

39	1KT18EE400	Write a note on encoders.	5	CO3	L2
40	1KT18EE401	What are the problem associated with the basic encoder explain how can these problems be overcome by priority encoder, considering 8-bit input lines.	5	CO2	L2
41	1KT17EE001	Realize the following Boolean functions using 74139. a) $f(w,x) = \sum m(0,2)$ b) $f(a,b,c) = \sum m(1,3,6,7)$.	5	CO3	L4
42	1KT17EE002	Configure a 16 to 1 MUX using 4 to 1 MUX.	5	CO3	L4
43	1KT17EE003	Design 2-bit comparator using gates	5	CO3	
44	1KT17EE005	Design a 4-bit BCD adder circuit using IC7483, with self correcting circuit. ie, a provision has to be made in the circuit, in case if the sum of BCD number exceeds 9.	5	CO4	L4
45	1KT17EE007	Design and implement a 4-bit look ahead carry adder.	7	CO4	L4
46	1KT17EE008	Implement a 12-bit comparator using IC7485.	5	CO4	
47	1KT17EE009	Design a comparator to check if two n-bit numbers are equal. Configure these using cascaded stages of 1-bit comparators.	5	CO4	L4
48	1KT17EE010	Design a binary full adder using minimum number of gates.	5	CO4	L4
49	1KT16EE003	Explain the following terms a)Ripple carry propagation b)Propagation delayc)Look ahead carry d)Iterative design.	7	CO4	L2
50	1KT16EE010	Design a binary full subtractor using minimum number of gates.	5	CO4	L4
51	1KT16EE005	Explain 4-bit Parallel adder and subtractor.	5	CO4	L2
52	1KT18EE400	Explain Decimal adder.	5	CO4	L2
53	1KT18EE401	Explain Decimal adder.	5	CO4	L2
54	1KT17EE001	Implement the following Boolean function with 8:1 multiplexer $f(a,b,c,d) = \sum m(0,2,6,10,11,12,13) + \sum d(3,8,14)$	7	CO3	L4
55	1KT17EE002	Design a full adder using MUX. For a full adder S= $\sum m(1,2,4,7)$ C = $\sum m(3,5,6,7)$	7	CO4	L4

D2. TEACHING PLAN - 2

Module - 3

Title:	Sequential Circuits	Appr Time:	16 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Understand the logics of Flip flops & Latches using Logic diagrams & verifying with truth table.	CO5	L2
2	Analyze & Design of counters using clocked D,T or SR flip flops.	CO6	L4

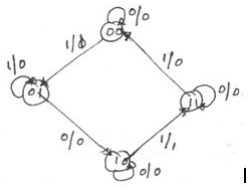
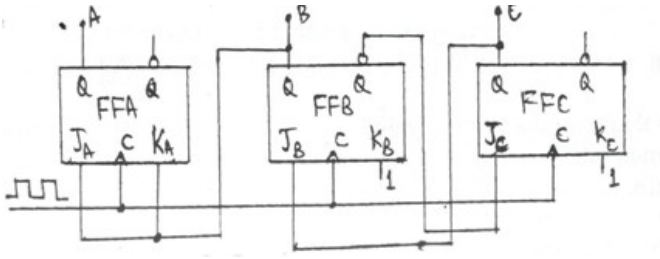
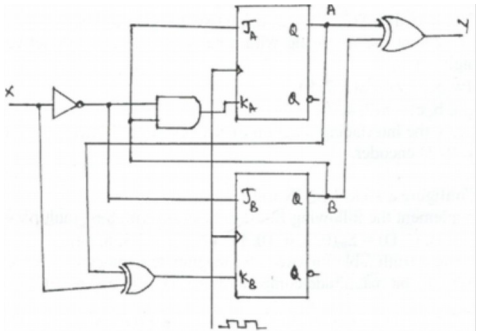
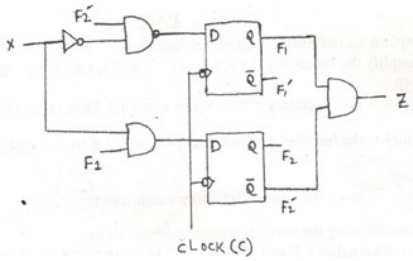
b	***Course Schedule***		
Class No	**Module Content Covered**	**CO**	**Level**
1	Basic Bistable element	CO5	L2
2	Latches, SR latch, application of SR latch	CO5	L2
3	A Switch debouncer	CO5	L2
4	The gated SR latch	CO5	L2
5	The gated D Latch	CO5	L2
6	The Master-Slave Flip-Flops (Pulse-Triggered Flip-Flops): The master-slave SR Flip-Flops	CO5	L2
7	The master-slave JK Flip-Flop	CO5	L2
8	Characteristic equations	CO6	L3
9	Registers	CO6	L2
10	Counters-Binary Ripple Counter	CO6	L2
11	Synchronous Binary counters	CO6	L2
12	Counters based on Shift Registers	CO6	L2
13	Design of a Synchronous counters	CO6	L4
14	Design of a Synchronous Mod-6 counters using clocked JK Flip-Flops	CO6	L4
15	Design of a Synchronous Mod-6 counter using clocked D, T, or SR Flip Flops	CO6	L4
c	**Application Areas**	**CO**	**Level**
1	In formation of Registers	CO5	L2
2	To Set an AC timer, Flashing indicator lights of your vehicle, etc	CO6	L4
d	**Review Questions**	-	-
1	Explain with timing diagram the working of SR Latch as a switch debouncer	CO5	L2
2	Explain the working of master slave JK flip flop with the functional table and timing diagram. Show how race around condition of master slave SR flip flop is overcome.	CO5	L2
3	What is the significance of edge triggering? Explain the working of edge triggered D - flip flop and T - Flip flop with their functional table.	CO5	L2
4	What is a Flip Flop? Discuss the working principle of SR Flip Flop with its truth table. Also highlight the role of SR Flip Flop in switch debouncer circuit	CO5	L2
5	With neat schematic diagram of master slave JK-FF, discuss its operation. Mention the advantages of JK-FF over master-slave SR-flip-flop .	CO5	L2
6	Clearly distinguish between	CO5	L2

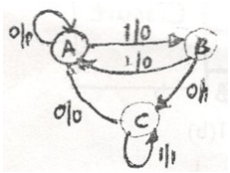
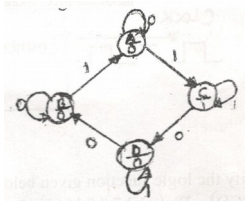
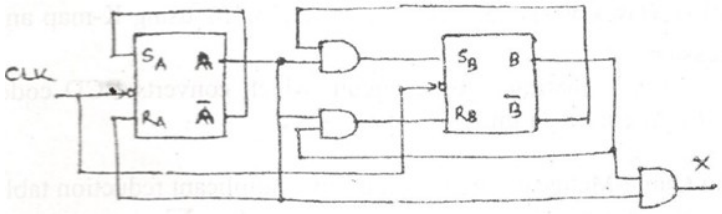
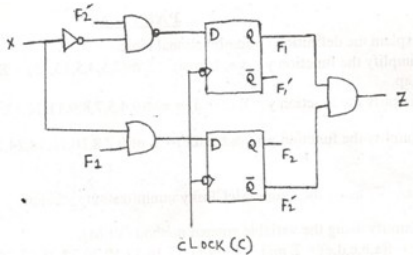
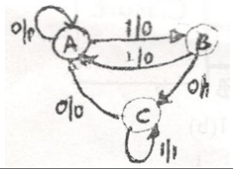
	a.Synchronous and asynchronous circuits. b.Combinational and sequential circuits		
7	Explain the operation of clocked SR flip-flop	CO5	L2
8	What is race around condition? Discuss in detail.	CO5	L2
9	Explain the operation of SR latch. Explain one of its applications	CO5	L2
10	What is the difference between a flip flop and a latch? What is gated SR Latch?	CO5	L2
11	Explain the operation of gated SR Latch, With a logic diagram, Truth table and logic symbol.	CO5	L2
12	Explain the operation of positive-edge-triggered JK flip-flop and T flip-flop, with the help of logic diagram, function table and logic symbol.	CO5	L2
13	Explain the following: a.Switch debouncing and its elimination. b.Race around problem and its elimination	CO5	L2
14	Explain basic bistable element	CO5	L2
15	Explain the problem of 0's and 1's catching in master slave JK flip-flop.	CO5	L2
16	Explain the operation of positive-edge-triggered D flip-flop and T flip-flop, with the help of logic diagram, function table and logic symbol.	CO5	L2
17	How do you convert JK flip-flop to SR flip-flop.	CO5	L3
18	What is meant by triggering of flip-flops? Name the different triggering methods.	CO5	L2
19	Explain the working of pulse triggered JK flip-flop with typical JK flip-flop waveforms.	CO5	L2
20	Derive the characteristics equations of SR and JK Flip Flops.	CO5	L3
21	With a neat circuit diagram, explain the working of a universal shift register.	CO6	L2
22	Design a synchronous MOD-6 counter using clocked JK FF.	CO6	L4
23	With neat diagram and counting sequence explain synchronous MOD-10 counter.	CO6	L2
24	With neat diagram and counting sequence explain 4-bit binary ripple Counter.	CO6	L2
25	Write the differences between Synchronous and Asynchronous counters.	CO6	L2
26	Design a synchronous MOD-5 counter using clocked JK FF.	CO6	L4
27	Derive the characteristics equations of D and T Flip Flops.	CO6	L3
28	Explain the working principle of mod-8 binary ripple counter, configured using positive edge triggered T-FF. also draw the timing diagram.	CO6	L2
29	Design Mod-6 synchronous counter using JK flip-flop	CO6	L4

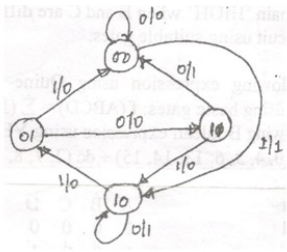
30	Design a synchronous counter to count from 0000 to 1001 using JK flip-flops	CO6	L4
31	Draw the circuit of a 3-bit asynchronous down counter using negative edge triggered JK flip-flops and draw the timing waveforms.	CO6	L2
32	Design and implement a synchronous counter to count the sequence 0-3-2-5-1-0 using negative edge triggered JK flip-flops.	CO6	L4
e	**Experiences**	-	-
1		CO1	L2
2			
3			
4		CO3	L3
5			

Module - 4

Title:	Sequential Design	Appr Time:	16 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Understand the Mealy & Moore models using their Block diagrams.	CO7	L2
2	Analyze & Design of Sequential circuits using State & state transition technique.	CO8	L4
b	***Course Schedule***		
Class No	**Module Content Covered**	**CO**	**Level**
1	Introduction	CO7	L2
2	Mealy and Moore models	CO7	L2
3	State machine notation	CO8	L2
4	synchronous sequential circuit analysis and design.	CO8	L4
5	Construction of state Diagrams	CO8	L4
6	Counters Design.	CO8	L4
c	**Application Areas**	**CO**	**Level**
1	To designing the sequential circuits.	CO7	L2
2	To design Elevator, vending machine, etc.	CO8	L4
d	**Review Questions**	-	-
1	Explain Mealy ad Moore sequential circuit models.	CO7	L2
2	Design a synchronous counter using JK flip-flops to convert the sequence 0,1,2,4,5,6,0,1,2. Use static diagram and state table	CO8	

3	Design a clocked sequential circuit that operates according to the state diagram shown. Implement the circuit using D flip-flop. 	CO8	L4
4	Compare mealy and moore models.	CO7	L2
5	Analyse the synchronous sequential circuit shown in the figure below. 	CO8	L4
6	Construct the excitation table, transition table, state table and state diagram for the Moore sequential circuit shown in figure. 	CO8	L4
7	For the logic diagram given in figure, a)Derive the excitation and output equations. b)Write the next state equations c)Construct a transition table and d)Draw the state diagram. 	CO8	L4

8	Construct the state table for the following state diagram  	CO8	L4
9	Give the output function, excitation table and state transition diagram by analyzing the sequential circuit shown in the figure below. 	CO8	L4
10	Construct the excitation table, transition table, state table and state diagram, for the Moore sequential circuit shown in the figure. 	CO8	L4
11	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with JK flip-flop. 	CO8	L4

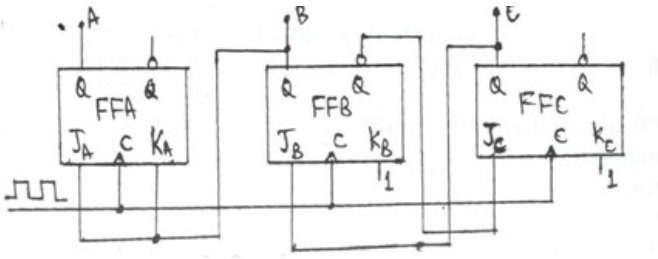
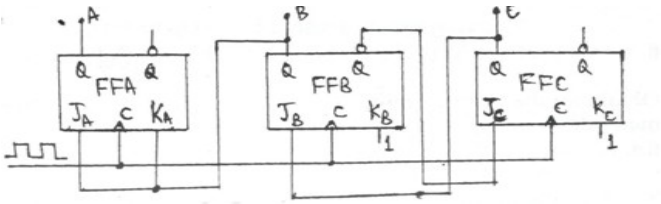
12	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with T flip-flop.  	CO8	L4
e	**Experiences**		
1			
2			
3			
4			
5			

E2. CIA EXAM – 2

a. Model Question Paper – 2

Crs Code:	17EE35	Sem:	III	Marks:	30	Time:	75 minutes
Course:	Design and Analysis of Algorithms						

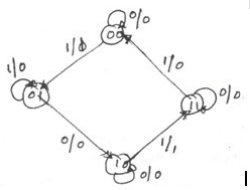
-	-	**Note: Answer any 2 questions, each carry equal marks.**	**Marks**	**CO**	**Level**
1	a	Explain the working of master slave JK flip flop with the functional table and timing diagram. Show how race around condition of master slave SR flip flop is overcome.	7	CO5	L2
	b	With neat schematic diagram of master slave JK-FF, discuss its operation. Mention the advantages of JK-FF over master-slave SR-flip-flop .	8	CO5	L2
2	a	Clearly distinguish between Synchronous and asynchronous circuits. combinational and sequential circuits.	7	CO5	L2
	b	Explain the working of pulse triggered JK flip-flop with typical JK flip-flop waveforms.	8	CO5	L2

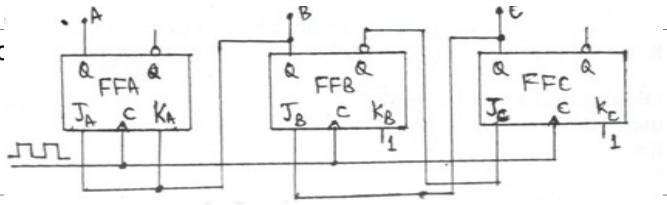
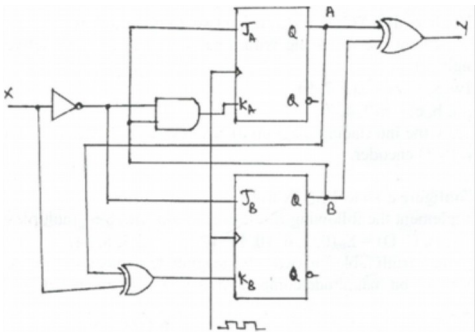
3	a	Explain Mealy ad Moore sequential circuit models.	7	CO7	L2
	b	Analyse the synchronous sequential circuit shown in the figure below. 	8	CO8	L4
4	a	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with JK flip-flop. 		CO8	L4
	b	Explain Mealy ad Moore sequential circuit models.	8	CO7	L2

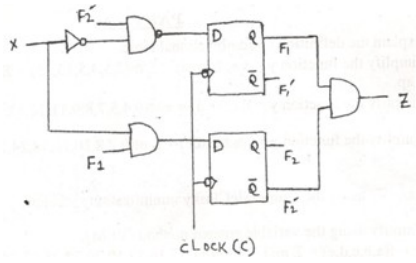
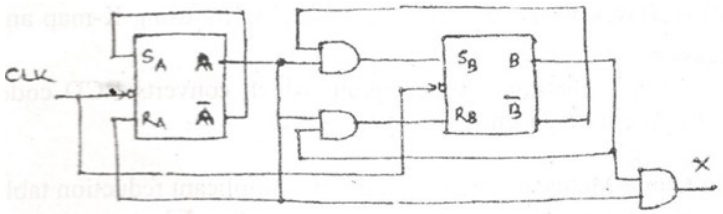
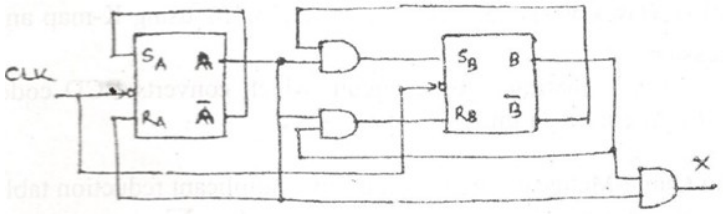
b. Assignment – 2

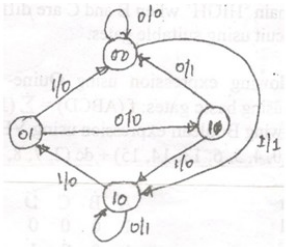
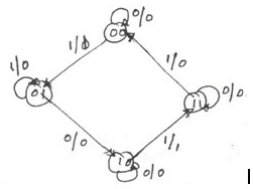
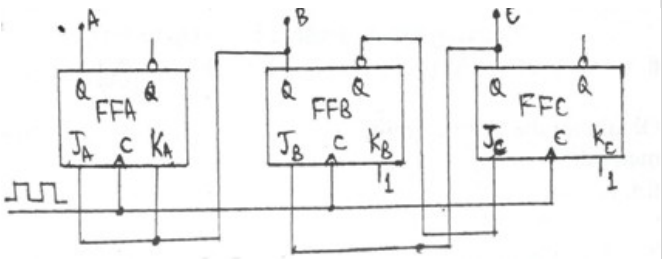
Note: A distinct assignment to be assigned to each student.

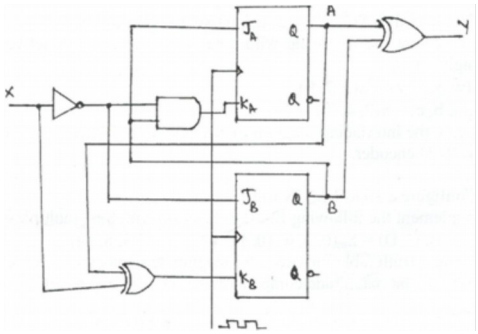
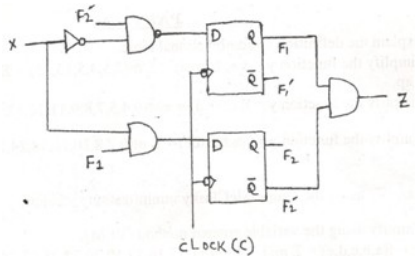
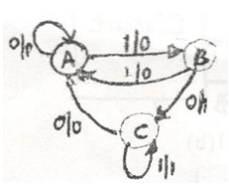
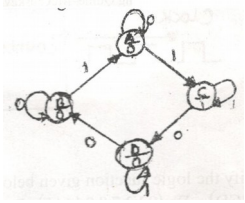
Model Assignment Questions							
Crs Code:	17EE35	Sem:	III	Marks:	10 / 10	Time:	90 – 120 minutes
Course:	Digital System Design						
Note: Each student to answer 2–3 assignments. Each assignment carries equal mark.							

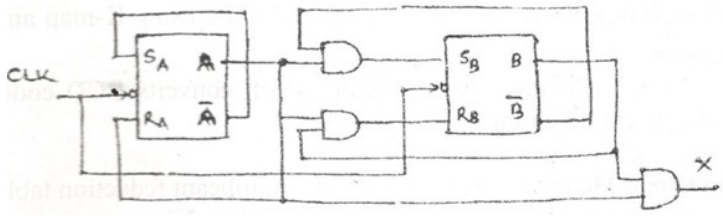
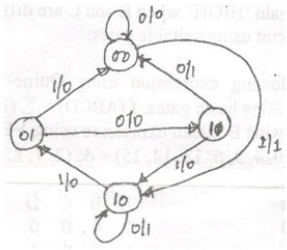
SNo	USN	Assignment Description	Marks	CO	Level
1	1KT17EE001	Explain Mealy ad Moore sequential circuit models.	8	CO7	L2
2	1KT17EE002	Design a synchronous counter using JK flip-flops to convert the sequence 0,1,2,4,5,6,0,1,2. Use static diagram and state table	6	CO8	
3	1KT17EE003	Design a clocked sequential circuit that operates according to the state diagram shown. Implement the circuit using D flip-flop. 	8	CO8	L4

4	1KT17EE005	Cc 	5	CO7	L2
5	1KT17EE007	Analyse the synchronous sequential circuit shown in the figure below.	8	CO8	L4
6	1KT17EE008	Construct the excitation table, transition table, state table and state diagram for the Moore sequential circuit shown in figure. 	8	CO8	L4

7	1KT17EE009	For the logic diagram given in figure, a)Derive the excitation and output equations. b)Write the next state equations c)Construct a transition table and d)Draw the state diagram.  	8	CO8	L4
8	1KT17EE010	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with JK flip-flop.	8	CO8	L4
9	1KT16EE003	Give the output function, excitation table and state transition diagram by analyzing the sequential circuit shown in the figure below.  	8	CO8	L4
10	1KT16EE010	Construct the excitation table, transition table, state table and state diagram, for the Moore sequential circuit shown in the figure.  	8	CO8	L4

11	1KT16EE005	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with JK flip-flop.	8	CO8	L4
12	1KT18EE400	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with T flip-flop. 	8	CO8	L4
13	1KT18EE401	Explain Mealy ad Moore sequential circuit models.	5	CO7	L2
14	1KT17EE001	Design a synchronous counter using JK flip-flops to convert the sequence 0,1,2,4,5,6,0,1,2. Use static diagram and state table	6	CO8	
15	1KT17EE002	Design a clocked sequential circuit that operates according to the state diagram shown. Implement the circuit using D flip-flop. 	8	CO8	L4
16	1KT17EE003	Compare mealy and moore models.	5	CO7	L2
17	1KT17EE005	Analyse the synchronous sequential circuit shown in the figure below. 	8	CO8	L4
18	1KT17EE007	Construct the excitation table, transition table, state table	8	CO8	L4

		and state diagram for the Moore sequential circuit shown in figure. 			
19	1KT17EE008	For the logic diagram given in figure, a)Derive the excitation and output equations. b)Write the next state equations c)Construct a transition table and d)Draw the state diagram. 	8	CO8	L4
20	1KT17EE009	Construct the state table for the following state diagram  	8	CO8	L4

21	1KT17EE010	Give the output function, excitation table and state transition diagram by analyzing the sequential circuit shown in the figure below. 	8	CO8	L4
22	1KT16EE003	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with T flip-flop. 	8	CO8	L4

D3. TEACHING PLAN - 3

Module - 5

Title:	HDL & Data-Flow Descriptions	Appr Time:	16 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Understand the structure of HDL, operators using block diagram & compare between VHDL & Verilog.	CO9	L2
2	Understand the structure of Data flow description using block diagram & flowchart.	CO10	L2
b	***Course Schedule***		
Class No	**Module Content Covered**	**CO**	**Level**
1	Introduction	CO9	L2
2	A brief history of HDL	CO9	L2
3	Structure of HDL Module	CO9	L2
4	Operators	CO9	L2
5	Data types	CO9	L2

6	Types of Descriptions (only VHDL)	CO9	L2
7	Simulation and synthesis	CO9	L2
8	Brief comparison of VHDL and Verilog	CO9	L2
9	Data-Flow Highlights of Data flow descriptions	CO10	L2
10	Structure of data-flow description	CO10	L2
c	**Application Areas**	**CO**	**Level**
1	Used for RTL or logic level description of any digital VLSI circuits.	CO9	L2
2		CO10	L2
d	**Review Questions**	-	-
1	Compare VHDL and Verilog		
2	Explicate the structure of verilog module.		
3	Given A = 1000 and B = 0011, perform the following operations: i) A XNOR B ii) Shift B two position left logical iii) Reduction NAND iv) Verilog concatenation {A,B} v) Verilog modules A%B.		
4	Describe scalar data type used in VHDL.		
5	Discuss logical and arithmetic operators used in VHDL.		
6	Elaborate any two data types used in verilog.		
7	Write behavioral description of the full adder circuit using VHDL and verilog.		
8	Write a switch level description in VHDL for the inverter circuit with nmos and pmos.		
e	**Experiences**	-	-
1			
2			
3			
4			
5			

E3. CIA EXAM – 3

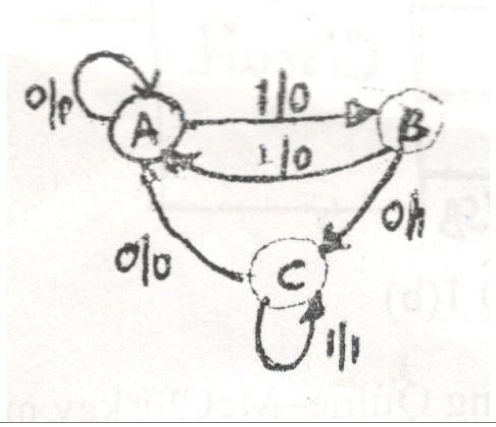
a. Model Question Paper – 3

Crs Code:	17EE35	Sem:	III	Marks:	30	Time:	75 minutes

EE

Prepared by Checked by Approved

Course: Design and Analysis of Algorithms

-	-	**Note: Answer any 2 questions, each carry equal marks.**	**Marks**	**CO**	**Level**
1	a	Write any two differences between mealy and moore model.	4	CO7	L2
	b	A sequential circuit has two flip-flops A and B, two inputs x and y, and an output Z. The flip-flop function and the circuit output functions are as follows: $J_A = xB + \overline{y}\overline{B}$; $K_A = x\overline{y}B$; $J_B = x\overline{A}$; $K_A = x\overline{y} + A$; $Z = xyA + \overline{x}\overline{y}B$ Write the excitation table and transition table for the same.	5	CO7	L4
	c	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with T flip-flop.	6	CO7	L4
		or			
2	a	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with T flip-flop.	5	CO7	L3
	b	Construct the state table for the following state diagram. 	5	CO7	L4
	c	Analyze the synchronous sequential circuit shown in the figure below.	5	CO7	L4
3	a	What are the steps to be followed for the design of sequential circuits?	5	CO7	L2
	b	Draw the state diagram of a Mealy machine to detect as input sequence 10110 with overlap. An output 1 is to be generated on when the sequence is detected.	5	CO8	L2

	c	Design a cyclic modulo-8 synchronous counter using T flip-flop that will count the number of occurrences of an input; that is, the number of times it is 1. The input variable X must be coincident with the clock to be counted. The counter is to count in binary.	5	CO8	L2
		or			
4	a	Explicate the structure of verilog module.	5	CO9	L
	b	Write a switch level description in VHDL for the inverter circuit with nmos and pmos.	5	CO9	L
	c	Discuss logical and arithmetic operators used in VHDL.	5	CO10	L

b. Assignment – 3

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions							
Crs Code:	17EE35	Sem:	I	Marks:	5 / 10	Time:	90 – 120 minutes
Course:	Design and Analysis of Algorithms						
Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.							

SNo	USN	Assignment Description	Marks	CO	Level
1	1KT17EE001	Compare VHDL and Verilog	4	CO5	L2
2	1KT17EE002	Explicate the structure of verilog module.	6	CO5	L2
3	1KT17EE003	Given A = 1000 and B = 0011, perform the following operations: i) A XNOR B ii) Shift B two position left logical iii) Reduction NAND iv) Verilog concatenation {A,B} v) Verilog modules A %B.	5	CO5	L4
4	1KT17EE005	Describe scalar data type used in VHDL.	5	CO5	L2
5	1KT17EE007	Discuss logical and arithmetic operators used in VHDL.	6	CO5	L2
6	1KT17EE008	Elaborate any two data types used in verilog.	4	CO5	L2
7	1KT17EE009	Write behavioral description of the full adder circuit using VHDL and verilog.	4	CO5	L2

8	1KT17EE010	Write a switch level description in VHDL for the inverter circuit with nmos and pmos.	6	CO5	L2

F. EXAM PREPARATION

1. University Model Question Paper

Course:	Digital System DEsign					Month / Year	Dec /2018
Crs Code:	17EE35	Sem:	3	Marks:	100	Time:	180 minutes

–	Note	Answer all FIVE full questions. All questions carry equal marks.	Marks	CO	Level
1	a	Explain combinational logic Circuit with the help of block diagram	5	C01	L2
	b	Define the following terms along with appropriate examples for better explanation a.Literal b.Minterm c.Maxterm d.Canonical SOP e.Canonical POS f.Normal SOP a. $f(X,Y,Z) = \sum(0,2,4,6) + dc(7)$ b. $f(X,Y,Z) = \prod(0,3,5,6).dc(7)$ c. $f(P,Q,R,S) = \sum m(0,1,4,8,9,10) + dc(2,11)$ d. $f(A,B,C,D) = \prod M(0,2,4,10,11,14,15)$	8	C01	L2
	c	Design a logic circuit that controls the passage of a signal 'A' according to the following requirement. a.Output 'X' will equal 'A' when control inputs B and C are the same. b.'X' will remain 'HIGH' when B and C are different. Implement the circuit using suitable gates	7	C02	L3
		OR			
1	a	Two motors M2 and M1 are controlled by three sensors S3, S2, S1. One motor M2 is to run any time all three sensors are on. The other motor is to run whenever sensors S2 or S1 but not both are on and S3 is off. For all sensor combinations where M1 is on, M2 is to be off except when all the three sensors are off and then both motors must remain off. Construct the truth table and write the Boolean output equation.	7	C01	L3
	b	Express the following SOP expressions into minterm list form and hence write maxterm list. a. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$ b. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$	6	C01	L3
	c	For the following Boolean function use the Quine Mc-Cluskey method to obtain all the prime implicants and apply Petrick's method to find the irredundant disjunctive normal expressions and identify the minimal sums. f(a, b, c, d) = $\sum m(4,5,7,12,14,15)$	7	CO2	L3
2	a	Two motors M2 and M1 are controlled by three sensors S3, S2, S1. One motor M2 is to run any time all three sensors are on. The other motor is to run whenever sensors S2 or S1 but not both are on and S3 is off. For all sensor combinations where M1 is on, M2 is to be off except when all the three sensors are off and then both motors must remain off. Construct the truth table and write the Boolean output equation.	7	C02	L3

	b	Implement the multiple functions: a)$f(a,b,c,d) = \sum m(0,4,8,10,14,15)$. b) $f(a,b,c,d) = \sum m(3,7,9,13)$. Using two 3 to 8 decoders.	6	CO3	L4
	c	Implement the following Boolean function with 8:1 multiplexer $f(a,b,c,d) = \sum m(0,2,6,10,11,12,13) + \sum d(3,8,14)$	7	CO4	L4
3	a	Explain the following: a.Switch debouncing and its elimination. b.Race around problem and its elimination	8	CO5	L2
	b	Derive the characteristics equations of SR and JK Flip Flops.	6	CO6	L3
	c	Derive the characteristics equations of D and T Flip Flops.	6	CO6	L3
4	a	Explain Switch debouncing and its elimination.	5	CO5	L2
	b	Analyze the synchronous sequential circuit shown in the figure below.	8	CO8	L4
	c	Explain Mealy and Moore Model with block diagram	7	CO8	L2
5	a	Compare VHDL and Verilog	5	CO9	L2
	b	Write a switch level description in VHDL for the inverter circuit with nmos and pmos.	7	CO9	L2
	c	Given A = 1000 and B = 0011, perform the following operations: i) A XNOR B ii) Shift B two position left logical iii) Reduction NAND iv) Verilog concatenation {A,B} v) Verilog modules A%B.	8	CO9	L3
		OR			
	a	Explicate the structure of verilog module.	6	C09	L2
	b	Describe scalar data type used in VHDL.	7	C10	L2
	c	Write behavioral description of the full adder circuit using VHDL and verilog.	7	CO10	L2

2. SEE Important Questions

Course:	Digital System DEsign					Month / Year	Dec /2018
Crs Code:	17EE35	Sem:	3	Marks:	100	Time:	180 minutes

	Note	Answer all FIVE full questions. All questions carry equal marks.	-	-	
Module	Qno.	Important Question	**Marks**	**CO**	**Year**

EE

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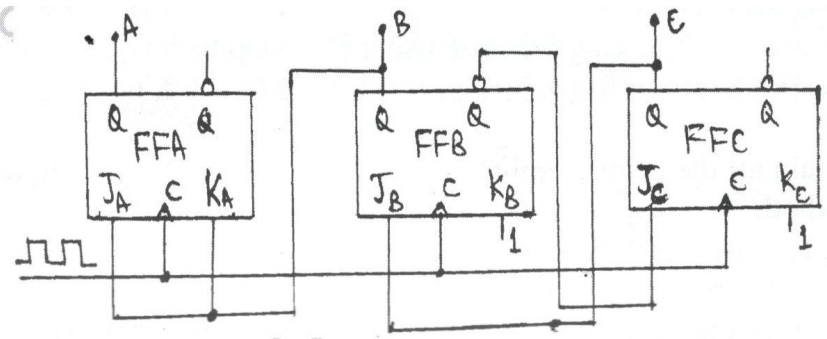
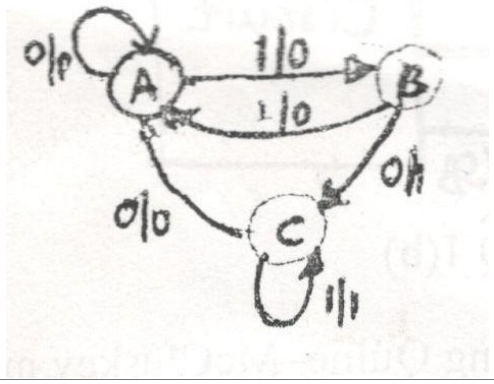
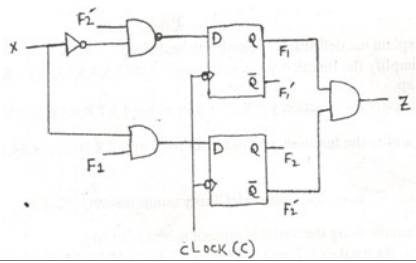
Design a full adder using MUX. For a full adder S= $\sum m(1,2,4,7)$ C = $\sum m(3,5,6,7)$

1	1	Explain combinational logic Circuit with the help of block diagram	5	C01	L2
	2	Define the following terms along with appropriate examples for better explanation a.Literal b.Minterm c.Maxterm d.Canonical SOP e.Canonical POS f.Normal SOP a. $f(X,Y,Z) = \sum(0,2,4,6) + dc(7)$ b. $f(X,Y,Z) = \prod(0,3,5,6).dc(7)$ c. $f(P,Q,R,S) = \sum m(0,1,4,8,9,10) + dc(2,11)$ d. $f(A,B,C,D) = \prod M(0,2,4,10,11,14,15)$	8	C01	L2
	3	Express the following SOP expressions into minterm list form and hence write maxterm list a. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$ b. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$	6	C01	L3
	4	Find all the Prime Implicants of the function f(a, b, c, d) = πM(0,2,3,4,5,12,13) + πd(8,10) using Quine Mc-Cluskey method.	8	C02	L2
	5	Two motors M2 and M1 are controlled by three sensors S3, S2, S1. One motor M2 is to run any time all three sensors are on. The other motor is to run whenever sensors S2 or S1 but not both are on and S3 is off. For all sensor combinations where M1 is on, M2 is to be off except when all the three sensors are off and then both motors must remain off. Construct the truth table and write the Boolean output equation.	7	C02	L3
2	1	Design a Combinational Circuit that accepts two unsigned 2-bit binary no. and provides 3 outputs. Inputs: A=A1A0 and B= B1B0 Output: A=B, A>B, A<B.	5	CO3	L4
	2	Implement the multiple functions: a) $f(a,b,c,d) = \sum m(0,4,8,10,14,15)$. b) $f(a,b,c,d) = \sum m(3,7,9,13)$. Using two 3 to 8 decoders.	5	CO3	L4
	3	Implement the following Boolean function with 8:1 multiplexer $f(a,b,c,d) = \sum m(0,2,6,10,11,12,13) + \sum d(3,8,14)$	5	CO4	L4
	4	Design and implement a 4-bit look ahead carry adder.	7	CO3	L4
	5	Design a comparator to check if two n-bit numbers are equal. Configure these using cascaded stages of 1-bit comparators.	5	CO4	L4
3	1	Explain the following: a.Switch debouncing and its elimination. b.Race around problem and its elimination	8	CO5	L2
	2	Explain basic bistable element	5	CO5	L2
	3	What is meant by triggering of flip-flops? Name the different triggering methods.	5	CO5	L2
	4	Derive the characteristics equations of SR and JK Flip Flops.	6	CO6	L3
	5	Derive the characteristics equations of D and T Flip Flops.	6	CO6	L3

4	1	Understand the Mealy & Moore models using their Block diagrams.	8	CO7	L2
	2	Analyze the synchronous sequential circuit shown in the figure below. 	8	CO8	L4
	3	Construct the state table for the following state diagram. 	10	CO7	L4
	4	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with JK flip-flop.	8	CO8	L4
	5	For the logic diagram given in figure, a)Derive the excitation and output equations. b)Write the next state equations c)Construct a transition table and d)Draw the state diagram. 	8	CO8	L4

5	1	Explicate the structure of verilog module.	5	C09	L2
	2	Describe scalar data type used in VHDL.	5	C10	L2
	3	Discuss logical and arithmetic operators used in VHDL.	6	CO5	L2
	4	Elaborate any two data types used in verilog.	4	CO5	L2
	5	Write behavioral description of the full adder circuit using VHDL and verilog.	4	CO5	L2
	6	Write a switch level description in VHDL for the inverter circuit with nmos and pmos.	6	CO5	L2