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# Table of Contents

18EE35 : Digital System Design	.2
A. COURSE INFORMATION	2
1. Course Overview	2
2. Course Content	2
3. Course Material	3
4. Course Prerequisites	4
B. OBE PARAMETERS	4
1. Course Outcomes	4
2. Course Applications	5
3. Articulation Matrix	6
4. Mapping Justification	7
5. Curricular Gap and Content	8
6. Content Beyond Syllabus	8
C. COURSE ASSESSMENT	9
1. Course Coverage	9
2. Continuous Internal Assessment (CIA)	9
D1. TEACHING PLAN – 1	9
Module – 1	9
Module – 2	13
E1. CIA EXAM - 1	16
a. Model Question Paper - 1	16
b. Assignment –1	17
D2. TEACHING PLAN – 2	21
Module – 3	21
Module – 4	23
E2. CIA EXAM – 2	26
a. Model Question Paper – 2	26
b. Assignment – 2	27
D3. TEACHING PLAN – 3	32
Module – 5	32
E3. CIA EXAM – 3	34
a. Model Question Paper – 3	34
b. Assignment – 3	35
F. EXAM PREPARATION	36
1. University Model Question Paper	36
2. SEE Important Questions	38

Note : Remove "Table of Content" before including in CP Book

AND TO THE CONTROL OF	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F02	Date:03-08-2018
	Title:	Course Plan	Page: 2 / 40

Each Course Plan shall be printed and made into a book with cover page

Blooms Level in all sections match with A.2, only if you plan to teach / learn at higher levels

# 18EE35 : Digital System Design

### A. COURSE INFORMATION

#### 1. Course Overview

Degree:	B.E	Program:	EE
Year / Semester :	3 <sup>rd</sup> / 3 <sup>rd</sup>	Academic Year:	2019-20
Course Title:	Digital System Design	Course Code:	18EE35
Credit / L-T-P:	3 / 4-0-0	SEE Duration:	180 Minutes
Total Contact Hours:	50	SEE Marks:	60 Marks
CIA Marks:	40	Assignment	1 / Module
Course Plan Author:	Kiranmayi M	Sign	Dt:03-08-2019
Checked By:		Sign	Dt:

### 2. Course Content

Mod	Module Content	Teaching	Module	Blooms
ule		Hours	Concepts	Level
1	Definition of combinational, canonical forms, Generation of		Combinationa	
	switching equations from truth tables, Karnaugh maps-3, 4		l circuits	
	and 5 variables. Incompletely specified functions (Don't care			
	terms). Simplifying max – term equations. Quine –McClusky	10		L2, L3
	minimization technique, Quine – McClusky using don't care			
	terms, Reduced Prime Implicant tables.		Boolean	
			algebra	
2	General approach, Decoders-BCD decoders, Encoders.		Boolean	
	Digital multiplexers-using multiplexers as Boolean function		function	
	generators. Adders and Subtractors-Cascading full adders,	10	generators	14
	Look ahead carry, Binary comparators. Design methods of	10		L4
	building blocks of combinational logics.		Ar-thematic	
			circuits	
3	Basic Bistable element, Latches, SR latch, application of SR	10		L2, L4
	latch, A Switch debouncer, The gated SR latch. The gated D		Flip flops	
	Latch, The Master-Slave Flip-Flops (Pulse-Triggered Flip-			

	SKIT	Teaching Process	Rev No.: 1.0			
Sign Na * 24 ArgaLone *	Doc Code:	SKIT.Ph5b1.F02	Date:03-08-2018			
	Title:	Course Plan	Page: 3 / 40			
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	Flops): The master-slave SR Flip-Flops, The master-slave JK			
	Flip-Flop. Characteristic equations, Registers, Counters-			
	Binary Ripple Counter, Synchronous Binary counters,			
	Counters based on Shift Registers, Design of a Synchronous			
	counters, Design of a Synchronous Mod-6 counters using			
	clocked JK Flip-Flops Design of a Synchronous Mod-6			
	counter using clocked D, T, or SR Flip Flops		Counters	
4	Introduction, Mealy and Moore models, State machine		State	
	notation, synchronous sequential circuit analysis and		machines	
	design. Construction of state Diagrams, Counters Design.	10		L2, L4
			Sequential	
			circuit design	
5	Introduction, A brief history of HDL, Structure of HDL		HDL	
	Module, Operators, Data types, Types of Descriptions (only			
	VHDL), Simulation and synthesis, Brief comparison of VHDL	10		1.2
	and Verilog.	10		LZ
	Data-Flow Highlights of Data flow descriptions, Structure of		data-flow	
	data-flow description		description	

### 3. Course Material

Mod	Details	Available
ule		
1	Text Books	
1.1	Digital Logic Applications, John M Yarbrough, CengageLearn, 2011	In Lib
1.2	Digital Principles and Design, Donald D, McGraw Hill, 1 <sup>st</sup> Edition, 2002	In Lib
2	Reference books	
2.1	Logic and computer design,Fundamentals, M. Morries Mano and Charles	
	Kime Pearson Learning 4 <sup>th</sup> , Edition, 2014	
2.2	Fundamentals of logic design, Charles H Roth, JR and Larry L.	
	Kinney,Cengage Learning 6 <sup>th</sup> Edition, 2013	
2.3	Fundamentals of Digital Circuits, A. Anand Kumar, PHI 3 <sup>rd</sup> Edition, 2014	
2.4	Digital Logic Design and VHDL, A.A.Phadke, S.M.Deokar, Wiley India 1 $^{ m st}$	
	Edition, 2009	
2.5	Digital Circuits and Design, D.P.KothariJ.S.Dhillon Pearson First Print 2015	
2.6	HDL Programming (VHDL and Verilog) Nazeih M. Botros Cengage	
	Learning1 Edition, 2011	
2.7	Circuit Design and Simulation with VHDL Volnei A Pedroni PHI 2 <sup>nd</sup> Edition	
3	Others (Web, Video, Simulation, Notes etc.)	
3.1	NPTL vedios	Available
3.2	Wikipedia	Available

ANNUAL STATE	UTE OF IRCH	SKIT	Teaching Process	Rev No.: 1.0
	*	Doc Code:	SKIT.Ph5b1.F02	Date:03-08-2018
	ALORE	Title:	Course Plan	Page: 4 / 40
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3.3	Writte	n notes		Available

#### 4. Course Prerequisites

SNo	Course	Course Name	Module / Topic / Description	Sem	Remarks	Blooms
	Code					Level
1	17ELN2	Basic Electronics	1. Knowledge Digital Electronics	2		L2
	4		Fundamentals			

Note: If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.

#### **B. OBE PARAMETERS**

#### 1. Course Outcomes

#	COs	Teach.	Concept	Instr	Assessmen	Blooms'
		Hours		Method	t Method	Level
18EE35.1	Understand the SOP & POS				Assignmen	
	expressions & their simplifications		Combinatio		t	L2
	from truth table.	5	nal circuits	Lecture	Unit Test	Understandi
					&	ng
					IA	
18EE35.2	Solving max terms of SOP & POS				Assignmen	
	using simplification techniques like		Boolean		t	13
	k-map, Quine -McClusky	8	algebra	Lecture	Unit Test	Apply
	minimization		aigebra		&	дрріу
	& Reduced Prime Implicant tables.				IA	
18EE35.3	Analyze & Design of Boolean				Assignmen	
	Expressions using Decoders &		Boolean		t	14
	Multiplexers.	7	function	Lecture	Unit Test	
			generators		&	Analyze
					IA	
18EE35.4	Analyze & Design of Adders & Subs				Assignmen	
	tractors using K-map		Ar–		t	1.4
		7	thematic	Lecture	Unit Test	
			circuits		&	Analyze
					IA	
18EE35.5	Understand the logics of Flip flops &	8	Flip flops	Lecture	Assignmen	L2
	Latches using Logic diagrams &				t	Understandi

MINITUTE CONTRACTOR	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F02	Date:03-08-2018
	Title:	Course Plan	Page: 5 / 40
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		8			Unit Test &	Analyze
					& IA	
18EE35.7	Understand the Mealy & Moore			Lecture	Assignmen	
	models using their block diagrams.	F	State		T Unit Tost	L2 Undorstandi
		5	machines		ent rest	na
					IA	ng
18EE35.8	Analyze & Design of Sequential			Lecture	Assignmen	
	circuits using State & state		Sequential		t	14
	transition technique.	8	circuit		Unit Test	L <del>4</del> Analyze
			design		&	Analyze
					IA	
18EE35.9	Understand the structure of HDL,		HDL	_	Assignmen	
	operators using block diagram &	-		Lecture	t Unit Tant	L2
	compare between VHDL & Verliog.	5		& DDT	Unit lest	Understandi
				PPI		ng
18FF35 1	Understand the structure of Data				Assianmen	
	flow description using block			Lecture	t	L2
0	now description using diock				-	
0	diagram & flowchart.	5	data-flow	&	Unit Test	Understandi
0	diagram & flowchart.	5	data-flow description	& PPT	Unit Test &	Understandi ng
0	diagram & flowchart.	5	data-flow description	& PPT	Unit Test & IA	Understandi ng

Note: Identify a max of 2 Concepts per Module. Write 1 CO per concept.

### 2. Course Applications

SNo	Application Area	CO	Level
1	Used in design of adder	CO1	L2
2	Automated Cafeteria	CO2	L3
3	To effective data exchange In communication system and to implement home	CO3	L4
	alarm system		
4	In forming ALU for desinging CPU to GPU	CO4	L4
5	In formation of Registers	CO5	L2
6	To Set an AC timer, Flashing indicator lights of your vehicle, etc	CO6	L4
7	To designing the sequential circuits & Can be used in video controller	C07	L2
8	To design Elevator, vending machine, etc.	CO8	L4

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		Title:	Course Plan P	age: 6 / 4	ge: 6 / 40					
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9 l	Used f	or chip desig	n and automation system	CO9	L2					
10 l	10 Used in transferring data.									

Note: Write 1 or 2 applications per CO.

#### 3. Articulation Matrix

#### (CO – PO MAPPING)

-	Course Outcomes	Program Outcomes												
#	COs	PO1	PO	PO	PO	PO	PO6	PO	PO	PO9	PO	PO	PO	Level
			2	3	4	5		7	8		10	11	12	
18EE35.1	Understand the SOP & POS expressions & their simplifications from truth table.	X												L2
18EE35.2	Solving max terms of SOP & POS using simplification techniques like k-map, Quine -McClusky minimization & Reduced Prime Implicant tables.	X	X											L3
18EE35.3	Analyze & Design of Boolean Expressions using Decoders & Multiplexers.	X	X	X										L4
18EE35.4	Analyze & Design of Adders & Subs tractors using K-map	Х		Х	Х									L4
18EE35.5	Understand the logics of Flip flops & Latches using Logic diagrams & verifying with truth table.		Х	Х	Х									L2
18EE35.6	Analyze & Design of counters using clocked D,T or SR flip flops.	Х		X	Х									L4
18EE35.7	Understand the Mealy & Moore models using their Block diagrams.	X												L2
18EE35.8	Analyze & Design of Sequential circuits using State & state transition technique.	X	X	X										L4
18EE35.9	Understand the structure of HDL, operators using block diagram & compare between	X		X										L2

	SKIT		Rev No.: 1.0					
Norodia	Doc Code:	SKIT.Ph5b1.F02				Date:03	8-08-	2018
SANGALORE	Title:	Course Plan				Page: 7	/ 40	
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	VHDL & Veri	log.						
18EE35.10	Understand	the structure of	Х	X				L2
	Data flow	description using						
	block diagra	m & flowchart.						
Note: Men	tion the ma	pping strength as	<b>1, 2, e</b>	or 3				

### 4. Mapping Justification

Мар	ping	Justification	Mapping
CO	PO		Level
C01	PO1	Applying the knowledge to simplify complex circuits.	L2
CO2	PO1	Knowledge of Boolean algebra helps the students in circuit designing	L3
CO2	PO2	Analysis of circuit provide the students for better understanding of digital circuits	L4
CO3	PO1	Its sound foundation to analyze digital circuits	L4
CO3	PO2	Choose a simplified circuit for implementing a combinational circuit using an appropriate simplification method	L2
CO3	PO3	Designing of complex combinational circuits	L4
CO4	PO1	This knowledge required to design mathematical circuits	L2
CO4	PO3	Designing of complex combinational circuits	L4
CO4	PO4	Choose a simplified circuit for implementing a combinational circuit using an appropriate simplification method	L2
CO5	PO2	Having knowledge in Flip flop and latches students could develop sequential circuit	L2
CO5	PO3	Knowledge of Flip flops could be used to reduce the complexity of the sequential circuit	L2
CO5	PO4	Having the knowledge in various sequential circuit design principles students could analyze the problem and come to a conclusion on which design principle to be use	L3
CO6	PO1	Knowledge in counter design helps to find solutions for complex engineering problems in digital electronics	L4
CO6	PO3	Knowledge in counter design helps digital electronics engineers to develop solutions for complex Engineering problems	L4
CO6	PO4	Choose a simplified circuit for implementing a Sequential circuit using an appropriate Flip flop.	L2
C07	PO1	An understanding state models helps to design automated machines.	L4
CO8	PO1	Knowledge in State Machines helps to find solutions for complex automated machines.	L2
CO8	PO2	Knowledge in State Machines helps to analyze complex automated machines	L4

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North International States	Doc Code: SKIT.Ph5b1.F02 Da								
SANGALORE	Title:	Course Plan	Page: 8						
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CO8	PO3	Basic principles of State Machines help to design a comp	lex	L2					
		utomated machine.							
CO9	PO1	Knowledge in HDL fundamentals help the students to do	)	L2					
		electronics program and digital logic circuits.							
CO9	PO3	Apply the suitable algorithms to design digital logic circu	Apply the suitable algorithms to design digital logic circuits						
CO10	PO1	nowledge required to know the flow of data graphically							
CO10	PO3	oply the suitable algorithms in data transferring							

Note: Write justification for each CO-PO mapping.

### 5. Curricular Gap and Content

SNo	Gap Topic	Actions	Schedule Planned	<b>Resources Person</b>	PO Mapping
		Planned			
1	Simulation Tools	Demo			
2	Practical use of number	Assignment			
	system				
3	Practical use of flip flops	Seminar			
4	Design of circuits	Practical			
5	Application of flip flops in	Practical			
	computers				

Note: Write Gap topics from A.4 and add others also.

### 6. Content Beyond Syllabus

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
5					
7					
8					
9					
10					

Note: Anything not covered above is included here.

### C. COURSE ASSESSMENT

#### 1. Course Coverage

Mod	Title	Teaching	No. of question in Exam					CO	Levels	
ule		Hours	CIA-	CIA-	CIA-	Asg	Extra	SEE		
#			1	2	3		Asg			

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A * SAI KR	A LOUIDA	Doc Code:	SKIT.Ph5b1.F0	2						Da	Date:03-08-2018			
1	NGALORE	Title:	Course Plan							Pa	Page: 9 / 40			
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1	1 Principles of			13	2	-	-	1	1	2	CO1,	L2, L3		
	combi	national logi	с								CO2			
2	Princip	oles of		14	2	-	-	1	1	2	CO3,	L4, L4		
	combi	national logi	с								CO4			
3	Seque	ntial Circuits		16	-	2	_	1	1	2	CO5,	L2, L4		
											CO6			
4	Seque	ntial		13	-	2	_	1	1	2	CO7,	L2, L4		
	Desigr	ı									C08			
5	HDL &	Data-Flow D	Descriptions	10	-	-	4	1	1	2	CO9,	L2, L2		
											CO10			
-		Tota	1	66	4	4	4	5	5	10	-	-		

Note: Distinct assignment for each student. 1 Assignment per chapter per student. 1 seminar per test per student.

#### 2. Continuous Internal Assessment (CIA)

Evaluation	Weightage in Marks	СО	Levels
CIA Exam - 1	30	CO1, CO2, CO3, CO4	L2, L3, L4, L4
CIA Exam - 2	30	CO5, CO6, CO7, C08	L2, L4, L2, L4
CIA Exam - 3	30	CO9, CO10	L2, L2
Assignment – 1	10	CO1, CO2, CO3, CO4	L2, L3, L4, L4
Assignment – 2	10	CO5, CO6, CO7, CO8	L2, L4, L2, L4
Assignment – 3	10	CO9, CO10	L2, L2
Seminar – 1			
Seminar – 2			
Seminar – 3			
Other Activities – define			
– Slip test			
<b>Final CIA Marks</b>	40	-	-

Note : Blooms Level in last column shall match with A.2 above.

### D1. TEACHING PLAN - 1

Title:	Principles of combinational logic	Appr	16 Hrs
		Time:	
а	Course Outcomes	_	Blooms
_	The student should be able to:	_	Level
1	Understand the SOP & POS expressions & their simplifications from truth table.	CO1	L2
2	Solving max terms of SOP & POS using simplification techniques like	CO2	L3

	SKIT	Teaching Process	Rev No	o.: 1.0
ABAN KHIS	Doc Code:	SKIT.Ph5b1.F02	Date:0	3-08-2018
4NGALORD	Title:	Course Plan	Page:	10 / 40
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	k-map, Quine	-McClusky minimization		
	& Reduced Pri	me implicant tables.		
b	Course Schedule			_
Class No	Module Conte	ent Covered	CO	Level
1	Definition of co	ombinational	C01	L2
2	canonical forms		CO1	L2
3	Generation of s	switching equations from truth tables,	CO1	L3
4	Karnaugh map	s-3, 4 and 5 variables.	CO2	L3
5	Incompletely s	pecified functions (Don't care terms).	CO2	L3
6	Simplifying ma	x – term equations.	CO2	L3
7	Quine –McClus	ky minimization technique,	CO2	L3
8	Quine – McClu	sky using don't care terms,	CO2	L3
9	Reduced Prime	Implicant tables.	CO2	L3
С	Application A	reas	СО	Level
1	To express the	boolean expressions	CO1	L2
2	To simplify the	Switching equations	CO2	L3
d	<b>Review Ques</b>	tions	_	_
1	Explain combina	ational logic Circuit with the help of block diagram	C01	L2
2	Define the folk explanation a.Literal b.Mint f.Normal SOP What are the dif	owing terms along with appropriate examples for better erm c.Maxterm d.Canonical SOP e.Canonical POS ferent ways of simplifying a Boolean expression	C01	L2
<u> </u>	What are canoni	ical forms illustrate with an example	C01	12
5	Reduce the follo	pwing function using K-Map technique and implement using	C01	13
	Basic gates.	a. $f(X,Y,Z) = \sum(0,2,4,6) + dc(7)$ b. $f(X,Y,Z) = \mathbb{II}(0,3,5,6), dc(7)$ c. $f(P,Q,R,S) = \sum m(0,1,4,8,9,10) + dc(2,11)$ d. $f(A,B,C,D) = \mathbb{II}M(0,2,4,10,11,14,15)$	COT	LJ
6	Reduce the follo	by bowing function using K-Map technique and implement using a. $f(A, B, C, D) = \sum (0,2,5,7,8,10,13,15) + dc(9,11)$ only the NAND b. $f(A, B, C, D) = \prod (3,4,6,11,12,14), dc(7,15)$ gates. c. $f(A, B, C, D) = \sum (1,3,4,6,9,11) + dc(5,7)$ d. $f(A, B, C, D) = \prod (0,1,2,5,9,11), dc(7,13)$	C01	L3
7	Convert the Sum $f(a, b, c) =$ b. $f(a, b, c) =$ c. $f(a, b, c) =$	of products expression to its Canonical form = $(ac + ab + bc)$ = $a. (abc)$ = $(ab' + bc)$	C01	L3

	SKIT	SKIT Teaching Process		Rev No.: 1.0	
Norder to the second se	Doc Code:	SKIT.Ph5b1.F02	Date:0	3-08-2018	
SANGALORE	Title:	Course Plan	Page:	11 / 40	
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8	Express the following write maxterm list	st	C01	L3	
	a. $f(a, b, c, d)$ b. $f(a, b, c, d)$	= (a b c + ab d + abcd + a b cd + abc'a) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)			
9	Design a logic c is zero or whene	ircuit with inputs P, Q, R so that output S is high whenever P ever Q=R=1	C01	L3	
10	Design a logic c majority of the ir	ircuit that has 4 inputs, the output will only be high, when the nputs are high, Use K – Map to simplify	C01	L3	
11	Design a logic c majority of the ir	ircuit that has 4 inputs, the output will only be high, when the nputs are high, Use K – Map to simplify	C01	L3	
12	Design a logic ci following require a.Output 'X' will b.'X' will remain using suitable ga	ircuit that controls the passage of a signal 'A' according to the ement. equal 'A' when control inputs B and C are the same. 'HIGH' when B and C are different. Implement the circuit ates	C01	L3	
13	Staircase light is other at the botto a.Make a truth ta form. c.Realize t minimum numbe	a controlled by two switches; one is at the top of the stair and om of the stairs. able for this system. b.Write the logic equations in the SOP the circuit using basic gates. Realize the circuit using er of NAND gates	C01	L3	
14	Design a combir code and draw t	national logic circuit, which converts BCD code into Excess-3 he circuit diagram.	C01	L3	
15	Distinguish bet Determine the s expression. $f(w, x, y, z) = \sum i$	ween prime implicants and essential prime implicants. ame of the function using K-map & hence the minimal sum m(0,1,4,5,9,11,13,15)	C01	L3	
16	Two motors M2 motor M2 is to r run whenever s sensor combina three sensors a truth table and w	and M1 are controlled by three sensors S3, S2, S1. One run any time all three sensors are on. The other motor is to ensors S2 or S1 but not both are on and S3 is off. For all tions where M1 is on, M2 is to be off except when all the re off and then both motors must remain off. Construct the vrite the Boolean output equation.	C01	L3	
17	Express the P notations) form b. $f(a, b, c, d) = (a + d)(a' + b + d)(a' + b + d)(a' + b + d)(a' + b)(a' + b)$	roduct of Sums equations in a maxterms list (decimal a. $f(a, b, c) = (a + b' + c)(a + b' + c)(a' + b' + c')$ a + b' + c + d)(a + b' + c + d')(a' + b + c + d)(a' + b' + c') c' + d)(a' + b' + c' + d)	C01	L3	
18	Convert the Prod a. $f(a, b, c) = ($ b. $f(a, b, c) = a$ c. $f(a, b, c) = ($	duct of Sums expression to its Canonical form (a+b)(b+c)(a+c) (a+b+c) (b+c)(ab'+c)	C01	L3	
19	Convert the Sun a. $f(a, b, c) =$ b. $f(a, b, c) =$ c. $f(a, b, c) =$	n of products expression to its Canonical form (ac + ab + bc) a. (abc) (ab' + bc)	C01	L3	
20	Express the fol write maxterm lis	lowing SOP expressions into minterm list form and hence st a. $f(a,b,c,d) = (abc + abd + abcd + abcd + abcd)$	C01	L3	
	Oliveral 11 1	$f(a, b, c, a) = (a \ b \ c + ab \ a + abca + ab \ ca + abc'a)$			
21	Simplify using $Q$ Y = f(a, b, c, d)	une McClusky tabulation algorithm = $\sum m(2,3,4,5,13,15) + dc(8,9,10,11)$	CO2	L3	

MUSTITUTE OF THE	SKIT	Teaching Process	Rev No.: 1.0	
Norder A	Doc Code:	SKIT.Ph5b1.F02	Date:0	3-08-2018
84NGALORE	Title:	Course Plan	Page:	12 / 40
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22	Simplify the logic fut technique. <i>Y</i> ( <i>A</i> , <i>B</i> , <i>C</i> , expression using unit	unction given below, using Quine - McClusky minimization $D = \sum m(0,1,3,7,8,11,15)$ . Realize the simplified versal gates.	CO2	L3
23	Using Quine McClusky method and prime implicant reduction table, Obtain the Minimal sum expression for the function			L3
24	Obtain the min technique. $Y =$	imal product of the following Boolean functions using (VEM) $f(a, b, c, d) = \sum m(1,5,7,10,11) + dc(2,3,6,13)$	CO2	L3
25	Simplify the fol implement using b	llowing expression using Quine-McClusky technique and asic gates. $f(A, B, C, D) = \sum m(1,3,4,5,6,9,11,12,13,14)$	CO2	L3
26	Minimize f(a, b, c, method.	d) = $\pi M(0,6,7,8,9,13) + \pi d(5,15)$ using Quine – McClusky	CO2	L3
27			CO2	L3
28	Find all the Prime $\pi$ d(8,10) using Qu	Implicants of the function $f(a, b, c, d) = \pi M(0,2,3,4,5,12,13) +$ tine Mc-Cluskey method.	CO2	L3
29	For the following all the prime im disjunctive norm $\sum m(4,5,7,12,14,2)$	Boolean function use the Quine Mc-Cluskey method to obtain plicants and apply Petrick's method to find the irredundant al expressions and identify the minimal sums. $f(a, b, c, d) = 15$ )	CO2	L3
30	Find a minimal sunction Quine $\Sigma d(4,11)$	Im for the following incomplete Boolean function using decimal Mc-cluskey method. $f(a, b, c, d) = \sum m(7,9,12,13,14,15) +$	CO2	L3
31	Write the map ente $\sum m(2,9,10,11,13,1)$	red variable K – Map for the Boolean function $f(w, x, y, z) =$ 44,15)	CO2	L3
32	Simplify using var basic gates. $f(a, b A'B'C'D' + A'B'C'D'$	iable entered mapping (VEM) technique and implement using a, c, d = A'B'C'D' + A'B'C'D + AB'C'D' + A'BC'D' + A'B'C'D' +	CO2	L3

MISTITUTE OF THE	SKIT	Teaching Process	Rev No.: 1.0
19010K	Doc Code:	SKIT.Ph5b1.F02	Date:03-08-2018
84NGALORE	Title:	Course Plan	Page: 13 / 40
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е	Experiences	-	-
1		CO1	L2
2			
3			
4		CO3	L3
5			

Title:	Analysis and design of Combinational Logic	Appr	10 Hrs
		Time:	
а	Course Outcomes	-	Blooms
-	The student should be able to:	-	Level
1	Analyze & Design of Boolean Expressions using Decoders & Multiplexers.	CO3	L4
2	Analyze & Design of Adders & Subs tractors using K-map	CO4	L4
b	Course Schedule	_	-
Class No	Module Content Covered	CO	Level
17	General approach	CO3	L2
18	Decoders-BCD decoders	CO3	L4
19	Encoders	CO3	L2
20	Digital multiplexers-using multiplexers as Boolean function generators.		L4
21	Adders and Subtractors-Cascading full adders	CO4	L3
22	Look ahead carry	CO4	L3
23	Binary comparators.	CO4	L4
24	Design methods of building blocks of combinational logics.	CO4	L4
С	Application Areas	СО	Level
1	To effective data exchange In communication system	CO3	L4
2	In forming ALU for desinging CPU to GPU	CO4	L4

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SKIT	Teaching Process	Rev No.: 1.0
Doc Code:	SKIT.Ph5b1.F02	Date:03-08-2018
Title:	Course Plan	Page: 14 / 40

d	Review Questions	-	-
1	Design a combinational logic circuit, which converts BCD code to Excess-3 code and draw the circuit diagram.	CO3	L4
2	Design a combinational logic circuit that will multiply two 2-bit binary values	CO3	L4
3	Design a combinational logic circuit to output the 2's complement of a 4-bit binary numbers: a) Construct the truth table. b) Simplify each output equation using K-map an write reduced equations. c) Draw the resulting logic diagram	CO3	L4
4	Design a combinational logic circuit to find 9's complement of a BCD number	CO3	L4
5	Design a combinational logic circuit to drive a common cathode seven segment display with BCD inputs	CO3	L4
6	Design a combinational logic circuit to output a 1 when an illegal BCD code occurs	CO3	L4
7	Design a combinational logic circuit to drive a common anode seven segment display with BCD inputs	CO3	L4
8	Design a Combinational Circuit that accepts two unsigned 2-bit binary no. and provides 3 outputs. Inputs: $A=A1A0$ and $B=B1B0$ Output: $A=B$ , $A>B$ , $A.$	CO3	L4
9	Develop the logic diagram of a 2 to 4 decoder with the following specifications: a)Active low enable input. b) Active high encoded outputs. Draw the IEEE symbol.	CO3	L3
10	Write the condensed truth table for 0,4, to 2 line priority encoder with a valid output where the highest priority is given to the highest bit position or input with highest index and obtain the minimal sum expressions for the outputs	CO3	L3
11	Describe the general working principle of decoder	CO3	L2
12	With the aid of block diagram, clearly distinguish between a decoder and encoder	CO3	L2
13	Implement a full subtractor using a decoder and NAND gates	CO4	L3
14	Design a logic circuit using a 3 to 8 logic decoder that has active low data inputs, an active HIGH enable and active low data outputs. Use such a decoder to realize the full adder circuit	CO4	L4
15	Designa 4 to 16 decoder using two 3 to 8 decoder (74LS138).	CO3	L4
16	Design a keypad interface to a digital system using ten line BCD encoder	CO3	L4
17	Implement a full adder using a decoder	CO3	L3
18	Implement 3-bit binary to gray code conversion by using IC 74139	CO3	L3
19	Design a priority encoder for a system with a 3 inputs, the middle bit with highest priority encoding to 10, the MSB with next priority encoding to 11, while the LSB with least priority encoding to 01	CO3	L4

	SKIT	Teaching Process	Rev No.:	1.0
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& MGALORE	Title:	Course Plan	Page: 15	i / 40
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20	Write a note or	n encoders.	CO3	L2
21	What are the p can these prob bit input lines.	problem associated with the basic encoder explain how plems be overcome by priority encoder, considering 8-	CO3	L2
22	Implement the r b) $f(a, b, c, d) =$	CO3	L4	
23	Implement the fo active high output	CO3	L4	
24	Realize the follow b) $f(a, b, c) = \sum r$	CO3	L4	
26	Configure a 16	to 1 MUX using 4 to 1 MUX.	CO3	L4
27	Design 2-bit comparator using gates		CO3	
28	Design a 4-bit circuit. ie, a pr of BCD numbe	CO4	L4	
29	Design and im	plement a 4-bit look ahead carry adder.	CO4	L4
30	Implement a 12	2-bit comparator using IC7485.	CO4	L3
31	Design a con Configure thes	nparator to check if two n-bit numbers are equal. e using cascaded stages of 1-bit comparators.	CO4	L4
32	Design a binar	y full adder using minimum number of gates.	CO4	L4
33	Explain the fol a)Ripple carry d)Iterative desi	lowing terms propagation b)Propagation delayc)Look ahead carry ign.	CO4	L2
34	Design a binar	y full subtractor using minimum number of gates.	CO4	L4
35	Explain 4-bit F	Parallel adder and subtractor.	CO4	L2
36	Explain Decim	al adder.	CO4	L2
37	Explain Decim	al adder.	CO4	L2
38	Implement the f	Following Boolean function with 8:1 multiplexer $f(a, b, c, d) = \sum m(0,2,6,10,11,12,13) + \sum d(3,8,14)$	CO3	L4
39	Design a full adder	using MUX. For a full adder S= $\sum m(1,2,4,7)$ C = $\sum m(3,5,6,7)$	CO4	L4
40	Implement the foll	owing function using 4:1 MUX $f(a, b, c) = \sum m(1,3,5,6)$	CO3	L4
е	Experiences		-	-
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## E1. CIA EXAM - 1

#### a. Model Question Paper - 1

Code:       Design and Analysis of Algorithms         -       Note: Answer any 3 questions, each carry equal marks.       M         1       a       Design a logical Circuit, when Two motors M2 and M1 are controlled by three sensors S3, S2 and S1. One motor M2 is to run any when all the three sensors are ON. The other motor is to run when ever sensors S2 or S1 but not both are ON and S3 is OFF. For all sensors	Mark s 5	<b>CO</b> 1	Level L3
<ul> <li>Note: Answer any 3 questions, each carry equal marks.</li> <li>A Design a logical Circuit, when Two motors M2 and M1 are controlled by three sensors S3, S2 and S1. One motor M2 is to run any when all the three sensors are ON. The other motor is to run when ever sensors S2 or S1 but not both are ON and S3 is OFF. For all sensors</li> </ul>	Mark s 5	<b>CO</b> 1	Level
1 a Design a logical Circuit, when Two motors M2 and M1 are controlled by three sensors S3, S2 and S1. One motor M2 is to run any when all the three sensors are ON. The other motor is to run when ever sensors S2 or S1 but not both are ON and S3 is OFF. For all sensors	5	C01 C01	L3
combinations where M1 is ON, M2 is OFF, except when all the three sensors are OFF and then both motors must remain OFF.	5	CO1	13
b Reduce the following functions using K-map technique and implement using Gates. (i) $f(P,Q,R,S) = \Sigma m (0,1,4,8,9,10)$ (ii) $f(A,B,C,D) = \Pi M (0,2,4,10,11,14,15)$			
c Express the following SOP expressions into minterm list form and hence write maxterm list a. $f(a, b, c, d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$ b. $f(a, b, c, d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$	5	CO1	L3
2 a Find a minimal sum for the following incomplete Boolean function using Decimal Q-M method and prime implicant table reduction $f(a,b,c,d) = \Sigma m (2,3,4,5,13,15) + \Sigma d (8,9,10,11)$	8	CO2	L3
b For a given incomplete Boolean function find a minimal sum & minimal product using MEV technique using A, B & C as map variables $F(A,B,C,D) = \Sigma m (1,5,6,7,9,11,12,13) + \Sigma d (0,3,4)$	7	CO2	L3
3 a Design 32:1 Multiplexer using only IC74150.	5	CO3	L4
b Design a combinational circuit to find 9,s complement of a BCD number, realize the circuit using suitable Logic gates.	5	CO3	L4
cRealizethefollowingBooleanfunction $P=f(w,x,y,z)$ $=\Sigma(0,1,5,6,7,10,15)$ using (i) 16 to 1 MUX (ii) 8 to 1 MUX (iii) 4 to 1 MUX	5	CO3	L3

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34	NGALORE	Title:	Course Plan	Page	: 17 / 4	40
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4	a	With a neat log	ic diagram, Explain Carry look ahead adder.	5	CO4	L2
	b	What is compa	arator? Design 2-bit comparator and implement with	5	CO4	L4
		suitable logic g	gates.			
	с	Write a note or	n encoders.	5	CO3	L3

# b. Assignment –1

Note: A distinct assignment to be assigned to each student.

				Мо	del Assignme	nt Questio	ns			
Crs	Code:	17EE35	Sem:	Ш	Marks:	5	Time:	90 - 120	) minu	tes
Cou	rse:	Design	and Analys	is of Alg	orithms					
Note	e: Each	studen	t to answer	2–3 assi	ignments. Eac	h assignm	ent carries equ	al mark.		
SN	U	SN		As	signment De	scription	l	Mark	CO	Level
1	1KT17	FF001	What are th	e differen	t ways of simpli	fying a Boc	lean expression	5	C01	12
2	16717	FF002	What are ca	anonical fo	orms illustrate v	/ith an exar	nple	5	C01	12
3	1KT17	EE003	Reduce th implement $f(X,Y)$ , b. $f(X,Y)$ , c. $f(P,Q)$ , d. $f(A,B)$ ,	e followin using Bas $Z) = \sum (0,2)$ $Z) = \prod (0,3)$ $R, S) = \sum n$ $C, D) = \prod N$	ng function us ic gates. 2,4,6) + dc(7) 3,5,6). dc(7) n(0,1,4,8,9,10) + d M(0,2,4,10,11,14,13)	sing K-Ma dc(2,11) (5)	p technique an	d 5	C01	L3
4	1KT17	EE005	Reduce th implement $f(A, B, B, b. f(A, B, c. f(A, B, d. f(A, B, $	e followin using only $C,D) = \sum(0,C,D) = \Pi(3,C,D) = \Pi(3,C,D) = \sum(1,C,D) = \Pi(0,C,D) = \Pi(0,C,D)$	ng function us the NAND gate ,2,5,7,8,10,13,15) + ,4,6,11,12,14). dc(7, ,3,4,6,9,11) + dc(5, ,1,2,5,9,11). dc(7,13)	sing K-Ma es. dc(9,11) (15) 7)	p technique an	d 5	C01	L3
5	1KT17	EE007	Convert the $f(a, b)$ b. $f(a, b)$ c. $f(a, b)$	Sum of pro (a, c) = (ac + b) $(a, c) = a \cdot (ab + b)$ (a, c) = (ab + b)	bducts expression + $ab + bc$ ) abc) + $bc$ )	to its Canor	nical form		C01	L3
6	1KT17	EE008	Express the hence write a. f(a, b, c, b. f(a, b, c,	e following maxterm (a'b'c - (a'b'c -	SOP expression list + ab'd + abcd + a'b' + ab'd + abcd + a'b'	cd + abc'd) cd + abc'd)	nterm list form an	d 5	C01	L3
7	1KT17	EE009	Design a lo 'A' accordi a.Output 'X the same. b.'X' will rer the circuit u	ogic circu ng to the X' will eq nain 'HIGI sing suita	iit that control following rec ual 'A' when c H' when B and o ble gates	s the pass juirement. ontrol inp C are differ	age of a signal uts B and C are ent. Implement	7	C01	L3
8	1KT17	EE010	Staircase li top of the a.Make a t equations gates. Rea	ght is co stair and ruth table in the SC lize the c	ntrolled by tw other at the b e for this syste P form. c.Real ircuit using m	o switches pottom of em. b.Write ize the cir inimum n	s; one is at the the stairs. e the logic cuit using basic umber of NAND	7	C01	L3

MISTITUTE OF THE	SKIT	Teaching Process	Rev No.: 1.0
Norock	Doc Code:	SKIT.Ph5b1.F02	Date:03-08-2018
SANGALORE	Title:	Course Plan	Page: 18 / 40
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		gates			
9	1KT16EE003	Design a combinational logic circuit, which converts BCD	7	C01	L3
		code into Excess-3 code and draw the circuit diagram.			
10	1KT16EE010	Distinguish between prime implicants and essential prime implicants. Determine the same of the function using K-map & hence the minimal sum expression. $f(w, x, y, z) = \sum m(0,1,4,5,9,11,13,15)$	7	C01	L3
11	1 KT16EE005	Two motors M2 and M1 are controlled by three sensors S3, S2, S1. One motor M2 is to run any time all three sensors are on. The other motor is to run whenever sensors S2 or S1 but not both are on and S3 is off. For all sensor combinations where M1 is on, M2 is to be off except when all the three sensors are off and then both motors must remain off. Construct the truth table and write the Boolean output equation.	7	C01	L3
12	1KT18EE400	Simplify the following expression using Quine-McClusky technique and implement using basic gates. $f(A, B, C, D) = \sum m(1,3,4,5,6,9,11,12,13,14)$	8	CO2	L3
13	1KT18EE401	Minimize $f(a, b, c, d) = \pi M(0, 6, 7, 8, 9, 13) + \pi d(5, 15)$ using Quine – McClusky method.	8	CO2	L3
15	1KT17EE001	Find all the Prime Implicants of the function $f(a, b, c, d) = \pi M(0,2,3,4,5,12,13) + \pi d(8,10)$ using Quine Mc-Cluskey method.	10	CO2	L3
16	1KT17EE002	For the following Boolean function use the Quine Mc-Cluskey method to obtain all the prime implicants and apply Petrick's method to find the irredundant disjunctive normal expressions and identify the minimal sums. $f(a, b, c, d) = \sum m(4,5,7,12,14,15)$	10	CO2	L3
17	1 KT1 7EE003	Find a minimal sum for the following incomplete Boolean function using decimal notation Quine Mc-cluskey method. $f(a, b, c, d) = \sum m(7,9,12,13,14,15) + \sum d(4,11)$	10	CO2	L3
18	1 KT1 7EE005	Write the map entered variable K – Map for the Boolean function $f(w, x, y, z) = \sum m(2,9,10,11,13,14,15)$	8	CO2	L3
19	1 KT1 7EE007	Simplify using variable entered mapping (VEM) technique and implement using basic gates. $f(a, b, c, d) = A'B'C'D' + A'B'C'D + AB'C'D' + A'BC'D' + A'B'C'D' + A'B'C'D'$	8	CO2	L3
20	1KT17EE008	Design a combinational logic circuit, which converts BCD	7	CO3	L4
		code to Excess-3 code and draw the circuit diagram.			
21	1 KT1 7EE009	Design a combinational logic circuit that will multiply two 2-bit binary values	5	CO3	L4
22	1 KT1 7EE010	Design a combinational logic circuit to output the 2's complement of a 4-bit binary numbers: a) Construct the truth table. b) Simplify each output equation using K-map an write reduced equations. c) Draw the resulting logic	5	CO3	L4

	SKIT	Teaching Process	Rev No.: 1.0
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MGALORE	Title:	Course Plan	Page: 19 / 40

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		diagram			
23	1KT16EE003	Design a combinational logic circuit to find 9's complement of a BCD number	5	CO3	L4
24	1KT16EE010	Design a combinational logic circuit to drive a common cathode seven segment display with BCD inputs	7	CO3	L4
25	1KT16EE005	Design a combinational logic circuit to output a 1 when an illegal BCD code occurs	5	CO3	L4
26	1KT18EE400	Design a combinational logic circuit to drive a common anode seven segment display with BCD inputs	7	CO3	L4
27	1KT18EE401	Design a Combinational Circuit that accepts two unsigned 2-bit binary no. and provides 3 outputs. Inputs: $A=A1A0$ and $B=B1B0$ Output: $A=B$ , $A>B$ , $A.$	7	CO3	L4
28	1KT17EE001	Develop the logic diagram of a 2 to 4 decoder with the following specifications: a)Active low enable input. b) Active high encoded outputs. Draw the IEEE symbol.	5	CO3	L3
29	1KT17EE002	Write the condensed truth table for 0,4, to 2 line priority encoder with a valid output where the highest priority is given to the highest bit position or input with highest index and obtain the minimal sum expressions for the outputs	5	CO3	L3
30	1KT17EE003	Describe the general working principle of decoder	5	CO3	L2
31	1 KT1 7EE005	With the aid of block diagram, clearly distinguish between a decoder and encoder	5	CO3	L2
32	1 KT1 7EE007	Implement a full subtractor using a decoder and NAND gates	5	CO4	L3
33	1 KT1 7EE008	Design a logic circuit using a 3 to 8 logic decoder that has active low data inputs, an active HIGH enable and active low data outputs. Use such a decoder to realize the full adder circuit	5	CO4	L4
34	1 KT1 7EE009	Designa 4 to 16 decoder using two 3 to 8 decoder (74LS138).	7	CO3	L4
35	1KT17EE010	Design a keypad interface to a digital system using ten line BCD encoder	7	CO3	L4
36	1KT16EE003	Implement a full adder using a decoder	5	CO3	L3
37	1KT16EE010	Implement 3-bit binary to gray code conversion by using IC 74139	5	CO3	L3
38	1 KT1 6EE005	Design a priority encoder for a system with a 3 inputs, the middle bit with highest priority encoding to 10, the MSB with next priority encoding to 11, while the LSB with least priority encoding to 01	7	CO3	L4

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39	IKII8	EE400	Write	a note on encoders.	5	CO3	L2
40	1KT18	EE401	What	are the problem associated with the basic encoder	5	CO2	L2
			expla	in how can these problems be overcome by priority			
			encod	der, considering 8–bit input lines.			
41	1KT17	EE001	Reali b) <i>f</i> (	ze the following Boolean functions using 74139. a) $f(w, x) = \sum m(0,2)$ $a, b, c) = \sum m(1,3,6,7).$	5	CO3	L4
42	1KT17	EE002	Confi	gure a 16 to 1 MUX using 4 to 1 MUX.	5	CO3	L4
43	1KT17	EE003	Desig	n 2-bit comparator using gates	5	CO3	
44			Desig	n a 4-bit BCD adder circuit using IC7483, with self	5	CO4	L4
			corre	cting circuit. ie, a provision has to be made in the			
	1KT17	EE005	circui	t, in case if the sum of BCD number exceeds 9.			
45	1KT17	EE007	Desig	n and implement a 4-bit look ahead carry adder.	7	CO4	L4
46	1KT17	EE008	Imple	ment a 12-bit comparator using IC7485.	5	CO4	
47	1KT17	EE009	Desig	n a comparator to check if two n-bit numbers are	5	CO4	L4
			equal	. Configure these using cascaded stages of 1-bit			
			comp	arators.			
48	1KT17	EE010	Desig	n a binary full adder using minimum number of	5	CO4	L4
			gates				
49	1KT16	EE003	Expla	in the following terms	7	CO4	L2
			a)Rip	ple carry propagation b)Propagation delayc)Look			
			ahead	d carry d)Iterative design.			
50	1KT16	EE010	Desig	n a binary full subtractor using minimum number of	5	CO4	L4
			gates	•			
51	1KT16	EE005	Expla	in 4-bit Parallel adder and subtractor.	5	CO4	L2
52	1KT18	EE400	Expla	in Decimal adder.	5	CO4	L2
53	1KT18	EE401	Expla	in Decimal adder.	5	CO4	L2
54	1KT17	EE001	Imple	ement the following Boolean function with 8:1 multiplexer	7	CO3	L4
				$f(a, b, c, a) = \underline{\geq} m(0, 2, 6, 10, 11, 12, 13) + \underline{\geq} a(3, 8, 14)$			
55	16212	FF002	Design	a full adder using MUX. For a full adder S= $\sum m(1,2,4,7)$ C = $\sum m(3.5.6.7)$	7	CO4	14
	/	22002			,	007	LT

# D2. TEACHING PLAN - 2

Title:	Sequential Circuits	Appr	16 Hrs
		Time:	
а	Course Outcomes	-	Blooms
-	The student should be able to:	-	Level
1	Understand the logics of Flip flops & Latches using Logic diagrams & verifying with truth table.	CO5	L2
2	Analyze & Design of counters using clocked D,T or SR flip flops.	CO6	L4

	SKIT	Teaching Process	Rev No.: 1.0
A BOTOK	Doc Code:	SKIT.Ph5b1.F02	Date:03-08-2018
S4NGALORE	Title:	Course Plan	Page: 21 / 40

	Course Schedule		
D			
Class No	Module Content Covered	CU	Levei
1	Basic Bistable element	CO5	L2
2	Latches, SR latch, application of SR latch	CO5	L2
3	A Switch debouncer	CO5	L2
4	The gated SR latch	CO5	L2
5	The gated D Latch	CO5	L2
6	The Master-Slave Flip-Flops (Pulse-Triggered Flip-Flops): The master-slave SR Flip-Flops	CO5	L2
7	The master-slave JK Flip-Flop	CO5	L2
8	Characteristic equations	CO6	L3
9	Registers	CO6	L2
10	Counters-Binary Ripple Counter	CO6	L2
11	Synchronous Binary counters	CO6	L2
12	Counters based on Shift Registers	CO6	L2
13	Design of a Synchronous counters	CO6	L4
14	Design of a Synchronous Mod-6 counters using clocked JK Flip-Flops	CO6	L4
15	Design of a Synchronous Mod-6 counter using clocked D, T, or SR	CO6	L4
	Flip Flops		
~			
<u> </u>	Application Areas	CO	Level
1	In formation of Registers	<b>CO</b> 5	Level L2
1 2	Application Areas In formation of Registers To Set an AC timer, Flashing indicator lights of your vehicle, etc	CO5 CO6	Level L2 L4
1 2 d	Application Areas         In formation of Registers         To Set an AC timer, Flashing indicator lights of your vehicle, etc         Review Questions	CO5 CO6	Level L2 L4
1 2 d	Application Areas         In formation of Registers         To Set an AC timer, Flashing indicator lights of your vehicle, etc         Review Questions         Explain with timing diagram the working of SR Latch as a switch debouncer	CO5 CO6 - CO5	Level L2 L4 - L2
1 2 d 1 2	Application Areas         In formation of Registers         To Set an AC timer, Flashing indicator lights of your vehicle, etc         Review Questions         Explain with timing diagram the working of SR Latch as a switch debouncer         Explain the working of master slave JK flip flop with the functional table and timing diagram. Show how race around condition of master slave SR flip flop is overcome.	CO5 CO6 - CO5 CO5	Level L2 L4 - L2 L2 L2
2 d 1 2 2 3	Application Areas         In formation of Registers         To Set an AC timer, Flashing indicator lights of your vehicle, etc         Review Questions         Explain with timing diagram the working of SR Latch as a switch debouncer         Explain the working of master slave JK flip flop with the functional table and timing diagram. Show how race around condition of master slave SR flip flop is overcome.         What is the significance of edge triggering? Explain the working of edge triggered D – flip flop and T – Flip flop with their functional table.	CO5 CO5 CO5 CO5	Level L2 L4 - L2 L2 L2
1       2       d       1       2       3       4	Application AreasIn formation of RegistersTo Set an AC timer, Flashing indicator lights of your vehicle, etcReview QuestionsExplain with timing diagram the working of SR Latch as a switch debouncerExplain the working of master slave JK flip flop with the functional table and timing diagram. Show how race around condition of master slave SR flip flop is overcome.What is the significance of edge triggering? Explain the working of edge triggered D – flip flop and T – Flip flop with their functional table.What is a Flip Flop? Discuss the working principle of SR Flip Flop with its truth table. Also highlight the role of SR Flip Flop in switch debouncer circuit	CO5 CO5 CO5 CO5 CO5	Level L2 L4 - L2 L2 L2 L2 L2
1       2       d       1       2       3       4       5	Application AreasIn formation of RegistersTo Set an AC timer, Flashing indicator lights of your vehicle, etcReview QuestionsExplain with timing diagram the working of SR Latch as a switch debouncerExplain the working of master slave JK flip flop with the functional table and timing diagram. Show how race around condition of master slave SR flip flop is overcome.What is the significance of edge triggering? Explain the working of edge triggered D – flip flop and T – Flip flop with their functional table.What is a Flip Flop? Discuss the working principle of SR Flip Flop with its truth table. Also highlight the role of SR Flip Flop in switch debouncer circuitWith neat schematic diagram of master slave JK-FF, discuss its operation. Mention the advantages of JK-FF over master-slave SR- flip-flop .	CO5 CO5 CO5 CO5 CO5 CO5	Level L2 L4 L2 L2 L2 L2 L2 L2 L2

Manual Long	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F02	Date:03-08-2018
	Title:	Course Plan	Page: 22 / 40

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	a.Synchronous and asynchronous circuits.		
	b.Combinational and sequential circuits		
7	Explain the operation of clocked SR flip-flop	CO5	L2
8	What is race around condition? Discuss in detail.	CO5	L2
9	Explain the operation of SR latch. Explain one of its applications	CO5	L2
10	What is the difference between a flip flop and a latch? What is gated SR Latch?	CO5	L2
11	Explain the operation of gated SR Latch, With a logic diagram, Truth table and logic symbol.	CO5	L2
12	Explain the operation of positive-edge-triggered JK flip-flop and T flip-flop, with the help of logic diagram, function table and logic symbol.	CO5	L2
13	Explain the following: a.Switch debouncing and its elimination. b.Race around problem and its elimination	CO5	L2
14	Explain basic bistable element	CO5	L2
15	Explain the problem of 0's and 1's catching in master slave JK flip- flop.	CO5	L2
16	Explain the operation of positive-edge-triggered D flip-flop and T flip-flop, with the help of logic diagram, function table and logic symbol.	CO5	L2
17	How do you convert JK flip-flop to SR flip-flop.	CO5	L3
18	What is meant by triggering of flip-flops? Name the different triggering methods.	CO5	L2
19	Explain the working of pulse triggered JK flip-flop with typical JK flip-flop waveforms.	CO5	L2
20	Derive the characteristics equations of SR and JK Flip Flops.	CO5	L3
21	With a neat circuit diagram, explain the working of a universal shift register.	CO6	L2
22	Design a synchronous MOD-6 counter using clocked JK FF.	CO6	L4
23	With neat diagram and counting sequence explain synchronous MOD-10 counter.	CO6	L2
24	With neat diagram and counting sequence explain 4-bit binary ripple Counter.	CO6	L2
25	Write the differences between Synchronous and Asynchronous counters.	CO6	L2
26	Design a synchronous MOD-5 counter using clocked JK FF.	CO6	L4
27	Derive the characteristics equations of D and T Flip Flops.	CO6	L3
28	Explain the working principle of mod-8 binary ripple counter, configured using positive edge triggered T-FF. also draw the timing diagram.	CO6	L2
29	Design Mod-6 synchronous counter using JK flip-flop	CO6	L4

	SKIT	Teaching Process	Rev No.:	1.0					
Noros	Doc Code:	SKIT.Ph5b1.F02	Date:03	-08-2018					
SANGALORE	Title:	Course Plan	Page: 23	8 / 40					
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30	Design a sync	hronous counter to count from 0000 to 1001 using JK	CO6	L4					
	flip-flops								
31	Draw the cir	cuit of a 3-bit asynchronous down counter using	CO6	L2					
	negative edge	triggered JK flip-flops and draw the timing waveforms.							
32	Design and im	plement a synchronous counter to count the sequence	CO6	L4					
	0-3-2-5-1-0	using negative edge triggered JK flip-flops.							
е	Experiences		-	_					
1			CO1	L2					
2									
3									
4			CO3	L3					
5									

Title:	Sequential	Appr	16 Hrs
	Design	Time:	
а	Course Outcomes	-	Blooms
-	The student should be able to:	-	Level
1	Understand the Mealy & Moore models using their Block diagrams.	C07	L2
2	Analyze & Design of Sequential circuits using State & state transition	CO8	L4
	technique.		
b	Course Schedule		
Class	Module Content Covered	CO	Level
No			
1	Introduction	C07	L2
2	Mealy and Moore models	C07	L2
3	State machine notation	CO8	L2
4	synchronous sequential circuit analysis and design.	CO8	L4
5	Construction of state Diagrams	CO8	L4
6	Counters Design.	CO8	L4
С	Application Areas	СО	Level
1	To designing the sequential circuits.	C07	L2
2	To design Elevator, vending machine, etc.	CO8	L4
d	Review Questions	_	-
1	Explain Mealy ad Moore sequential circuit models.	C07	L2
2	Design a synchronous counter using JK flip-flops to convert the	CO8	
	sequence 0,1,2,4,5,6,0,1,2. Use static diagram and state table		

	SKIT	Teaching Process	Rev No.:	1.0
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4NGALORE	Title:	Course Plan	Page: 24	/ 40
Copyright ©201	7. cAAS. All rights reser	ved.	C08	1.4
C	state diagram	008	L4	
4	Compare mea	ly and moore models.	C07	L2
5	Analyse the sy	Prochronous sequential circuit shown in the figure below. A A FFA $J_A$ C $K_A$ $T_B$ C $K_B$ $T_B$ $T_B$ C $K_B$ $T_B$	CO8	L4
0	diagram for th	e Moore sequential circuit shown in figure.	08	L4
7	For the logic c a)Derive the equations c)Co	liagram given in figure, excitation and output equations. b)Write the next state construct a transition table and d)Draw the state diagram. $\begin{array}{c} F_{2} \\ \hline \\ \hline \\ F_{2} \\ \hline \\ $	CO8	L4

	SKIT	Rev No.: 1.0		
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INGALO	Title:	Course Plan	Page: 25	/ 40
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8	Construct the	state table for the following state diagram	CO8	L4
	010			
9	Give the output by analyzing t	ut function, excitation table and state transition diagram he sequential circuit shown in the figure below.	CO8	L4
10	Construct the diagram, for th	excitation table, transition table, state table and state the Moore sequential circuit shown in the figure. $\begin{array}{c} & & & \\ & &$	CO8	L4
11	A sequential c as shown in th	ircuit has one output and one input, the state diagram is e figure. Design the sequential circuit with JK flip-flop.	CO8	L4

MILITUTE CONSCIONAL CO	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F02	Date:03-08-2018
	Title:	Course Plan	Page: 26 / 40

12	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with T flip-flop.	CO8	L4
е	Experiences		
1			
2			
3			
4			
5			

### E2. CIA EXAM - 2

## a. Model Question Paper - 2

Crs Cod	e:	17EE35	Sem:		Marks:	30	Time:	75	minutes		
Cou	rse:	Design ar	nd Analysis	s of Algori	thms						
-	-	Note: An	Note: Answer any 2 questions, each carry equal marks.								
1	a	Explain th table and slave SR f	xplain the working of master slave JK flip flop with the functional able and timing diagram. Show how race around condition of master slave SR flip flop is overcome.							CO5	L2
	b	With neat operation flip-flop	With neat schematic diagram of master slave JK-FF, discuss its operation. Mention the advantages of JK-FF over master-slave SR- flin-flop								L2
2	a	Clearly di combinat	Clearly distinguish between Synchronous and asynchronous circuits. combinational and sequential circuits.						7	CO5	L2
	b	Explain the working of pulse triggered JK flip-flop with typical JK flip- flop waveforms.						flip-	8	CO5	L2

MA INS		SKIT	Teaching Process	Rev	No.: 1.(	)
SIRI KRIS		Doc Code:	SKIT.Ph5b1.F02	Date	:03-08	-2018
BA	WGALORE	Title:	Course Plan	Page	: 27 / 4	40
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3	а	Explain Mealy	ad Moore sequential circuit models.	7	C07	L2
	b	Analyse the sy	nchronous sequential circuit shown in the figure below. FFA $R$ $FFB$ $R$ $FFC$ $R$ $R$ $FFC$ $R$ $FFC$ $R$ $FFC$ $R$ $FFC$ $R$ $FFC$ $R$ $R$ $R$ $FFC$ $R$	8	CO8	L4
4	a	A sequential cr as shown in the $T_{k} \in k$	ircuit has one output and one input, the state diagram is e figure. Design the sequential circuit with JK flip-flop.		CO8	L4
	b	Explain Mealy	ad Moore sequential circuit models.	8	C07	L2

## b. Assignment - 2

Note: A distinct assignment to be assigned to each student.

				Мос	del Assignme	nt Question	s				
Crs C	Code:	17EE35	Sem:	III	Marks:	10 / 10	Time:	90 - 120	0 - 120 minutes		
Cour	se:	Digital S	System De	sign							
Note	: Each	student	to answer	2–3 assig	gnments. Eacl	n assignmei	nt carries equ	al mark.			
SNo	L	JSN		As	signment De	scription		Mark	СО	Level	
								S			
1	1KT1	7EE001	Explain M	ealy ad Mo	oore sequenti	al circuit m	odels.	8	C07	L2	
2	1KT1	7EE002	Design a	synchro	nous counte	r using JK	flip-flops	to 6	CO8		
			convert th	e sequen	ce 0,1,2,4,5,6	5,0,1,2. Use	static diagra	m			
			and state	table							
3	1KT1	7EE003	Design a c	clocked se	quential circu	it that oper	ates accordir	ng 8	CO8	L4	
			to the stat	te diagran	n shown. Imp	lement the	circuit using	D			
					110 000						
				10	1	000					
						) /-					
					0000						



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dano	GALORE	Titl	e:	Course Plan	Page	e: 29 /	40		
Copyrigh 7	nt ©2017.	7EE009	hts reserv For the algorithm of the second s	the logic diagram given in figure, rive the excitation and output equations. b)Write the state equations c)Construct a transition table and aw the state diagram. $\mathbf{x} = \mathbf{x} + \mathbf{x} +$	8	CO8	L4		
8	1KT17	7EE010	A sec diagr circu	quential circuit has one output and one input, the state ram is as shown in the figure. Design the sequential it with JK flip-flop.	8	CO8	L4		
9	1KT16	5EE003	Give trans show	the output function, excitation table and state ition diagram by analyzing the sequential circuit in in the figure below.	8	CO8	L4		
10	1KT16	5EE010	Cons and s in the	truct the excitation table, transition table, state table state diagram, for the Moore sequential circuit shown e figure. $\qquad \qquad $	8	CO8	L4		

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SANGALORE	Title:	Course Plan	Page: 30 / 40				
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11	1KT16EE005	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with JK flip-flop.	8	CO8	L4
12	1 KT18EE400	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with T flip-flop.	8	CO8	L4
13	1KT18EE401	Explain Mealy ad Moore sequential circuit models.	5	C07	L2
14	1 KT1 7EE001	Design a synchronous counter using JK flip-flops to convert the sequence 0,1,2,4,5,6,0,1,2. Use static diagram and state table	6	CO8	
15	1 KT1 7EE002	Design a clocked sequential circuit that operates according to the state diagram shown. Implement the circuit using D flip-flop.	8	CO8	L4
16	1KT17EE003	Compare mealy and moore models.	5	C07	L2
17	1 KT 1 7EE005	Analyse the synchronous sequential circuit shown in the figure below. $ \begin{array}{c}                                     $	8	CO8	L4
18	1KT17EE007	Construct the excitation table, transition table, state table	8	CO8	L4



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SAM	GALORE	Title:	Course Plan	Page: 32 / 40		10	
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21		show	sition diagram by analyzing the sequential circuit which in the figure below.	0	0.0	L4	
22	1 KT1 (	5EE003 A se diagi circu	quential circuit has one output and one input, the state ram is as shown in the figure. Design the sequential at with T flip-flop.	8	CO8	L4	

## D3. TEACHING PLAN – 3

Title:	HDL & Data-Flow Descriptions	Appr	16 Hrs
		Time:	
а	Course Outcomes	-	Blooms
_	The student should be able to:	-	Level
1	Understand the structure of HDL, operators using block diagram & compare between VHDL & Verilog.	CO9	L2
2	Understand the structure of Data flow description using block diagram & flowchart.	CO10	L2
b	Course Schedule		
Class No	Module Content Covered	СО	Level
1	Introduction	CO9	L2
2	A brief history of HDL	CO9	L2
3	Structure of HDL Module	CO9	L2
4	Operators	CO9	L2
5	Data types	CO9	L2

	SKIT	SKIT Teaching Process							
A BOUNDARY	Doc Code:	SKIT.Ph5b1.F02	Date:03-	-08-2018					
&ANGALORE	Title:	Course Plan	Page: 33	/ 40					
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6	Types of Descr	iptions (only VHDL)	CO9	L2					
7	Simulation and	synthesis	CO9	L2					
8	Brief comparis	on of VHDL and Verilog	CO9	L2					
9	Data-Flow Hig	hlights of Data flow descriptions	CO10	L2					
10	Structure of da	ta-flow description	CO10	L2					
C	Application A	Areas	CO	Level					
1	Used for RTL o	r logic level description of any digital VLSI circuits.	CO9	L2					
2			CO10	L2					
d	Review Ques	tions	-	-					
1	Compare VHD	DL and Verilog							
2	Explicate the s	tructure of verilog module.							
3	Given A = 100 XNOR B ii) Shift B two concatenation	0 and B = 0011, perform the following operations: i) A position left logical iii) Reduction NAND iv) Verilog $\{A, B\}$ , v) Verilog modules $A\%B$							
4	Describe scalar	r data type used in VHDL							
5	Discuss logical	and arithmetic operators used in VHDL							
6	Elaborate any 1	two data types used in verilog							
		the data types used in ternog.							
7	Write behavior verilog.	ral description of the full adder circuit using VHDL and							
8	Write a switch nmos and pmo	level description in VHDL for the inverter circuit with s.							
е	Experiences		_	-					
1									
2									
3									
4									
5									
L									

# E3. CIA EXAM - 3

# a. Model Question Paper - 3

Crs	17EE35	Sem:	III	Marks:	30	Time:	75 minutes
Code:							

	SKIT	Teaching Process	Rev No.: 1.0
Norrow A	Doc Code:	SKIT.Ph5b1.F02	Date:03-08-2018
ANGALORE	Title:	Course Plan	Page: 34 / 40

Cou	rse:	Design and Analysis of Algorithms			
-	-	Note: Answer any 2 questions, each carry equal marks.	Mark s	CO	Level
1	a	Write any two differences between mealy and moore model.	4	C07	L2
	b	A sequential circuit has two flip-flops A and B, two inputs x and y, and an output Z. The flip-flop function and the circuit output functions are as follows:	5	C07	L4
		$J_A = xB + yB$ ; $K_A = xyB$ ; $J_B = xA$ ; $K_A = xy+A$ ; $Z = xyA + xyB$ Write the excitation table and transition table for the same.			
	c	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with T flip-flop.	6	C07	L4
		or			
2	a	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with T flip-flop.	5	C07	L3
	b	Construct the state table for the following state diagram.	5	C07	L4
	С	Analyze the synchronous sequential circuit shown in the figure below.	5	C07	L4
3	a	What are the steps to be followed for the design of sequential circuits?	5	C07	L2
	b	Draw the state diagram of a Mealy machine to detect as input sequence 10110 with overlap. An output 1 is to be generated on when the sequence is detected.	5	CO8	L2

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34	NGALORE	Title:	Course Plan	Page: 35 / 40		
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	с	Design a cycli will count the of times it is 1. to be counted.	c modulo-8 synchronous counter using T flip-flop that number of occurrences of an input; that is, the number The input variable X must be coincident with the clock The counter is to count in binary.	5	CO8	L2
			or			
4	а	Explicate the s	tructure of verilog module.	5	CO9	L
	b	Write a switch nmos and pmo	level description in VHDL for the inverter circuit with s.	5	CO9	L
	с	Discuss logical	and arithmetic operators used in VHDL.	5	CO10	L

## b. Assignment - 3

Note: A distinct assignment to be assigned to each student.

			Model	Assignment	Question	S			
Crs C	Code: 17EE	35 Sem:	I	Marks:	5 / 10	Time:	90 - 120	) minu	tes
Cour	se: Desig	n and Analysis	of Algorit	hms					
Note	: Each stude	nt to answer 2	–3 assignr	nents. Each	assignmer	nt carries equa	al mark.		
SNo	USN		Assignment Description						Level
							S		
1	1KT17EE00	1 Compare VI	Compare VHDL and Verilog						L2
2	1KT17EE00	2 Explicate the	e structure		6	CO5	L2		
3	1 KT1 7EE00	3 Given A = operations: i ii) Shift B iv) Verilog %B.	iven A = 1000 and B = 0011, perform the followin berations: i) A XNOR B ) Shift B two position left logical iii) Reduction NAN ) Verilog concatenation {A,B} v) Verilog modules						L4
4	1 KT1 7EE00	Describe sca	lar data ty	pe used in V	HDL.		5	CO5	L2
5	1KT17EE00	7 Discuss logi	cal and ari	thmetic oper	ators used	l in VHDL.	6	CO5	L2
6	1 KT1 7EE00	8 Elaborate an	y two data	types used	in verilog.		4	CO5	L2
7	1 KT1 7EE00	9 Write behav VHDL and v	ioral descr verilog.	ription of th	e full adde	er circuit usin	g 4	CO5	L2

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SANG	ALORE	Title	e:	Course Plan	Pag	Page: 36 / 40		
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8 1KT17EE010 W ci		Write circu	e a switch level description in VHDL for the inverter it with nmos and pmos.	6	CO5	L2		

### F. EXAM PREPARATION

### 1. University Model Question Paper

Cou	rse:	Digital System	Month	/ Year	Dec /2	2018				
Crs	Code:	17EE35	Sem:	3	Marks:	100	Time:		180	
									minut	es
_	Note	Answer all FIV	E full questic	ons. All ques	tions carry	equal marks		Mark	СО	Leve
								S		
1	a	Explain combination	ational logic C	ircuit with the	help of bloc	ck diagram		5	C01	L2
	b	Define the foll explanation a.Literal b.Min f.Normal SOP	Define the following terms along with appropriate examples for better explanation i.Literal b.Minterm c.Maxterm d.Canonical SOP e.Canonical POS .Normal SOP a. $f(X,Y,Z) = \sum (0,2,4,6) + dc(7)$ b. $f(X,Y,Z) = \prod (0,3,5,6), dc(7)$ c. $f(P,Q,R,S) = \sum m(0,1,4,8,9,10) + dc(2,11)$ d. $f(A,B,C,D) = \prod M(0,2,4,10,11,14,15)$							L2
	С	Design a logic of the following red a.Output 'X' will b.'X' will remain using suitable g	circuit that cor quirement. equal 'A' whe 'HIGH' when ates	trols the pass in control inpu B and C are o	age of a sig Its B and C a different. Im	nal 'A' accordi are the same. plement the cir	ng to rcuit	7	C02	L3
				OR						
1	a	Two motors M2 motor M2 is to run whenever s sensor combina three sensors a truth table and v	2 and M1 are run any time sensors S2 of ations where are off and th write the Boole	e controlled by all three sens r S1 but not I M1 is on, M2 en both moto ean output eq	y three sen sors are on. both are on 2 is to be o rs must ren uation.	sors S3, S2, The other mo and S3 is of ff except whe nain off. Cons	S1. One otor is to f. For all n all the truct the	7	C01	L3
	b	Express the following SOP expressions into minterm list form and hence write maxterm list. a. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$ b. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$						6	C01	L3
	С	For the following all the prime in disjunctive norm $\sum m(4,5,7,12,14,$	g Boolean func nplicants and nal expressions 15)	ation use the Quapply Petrick's and identify	uine Mc-Clus s method to the minima	skey method to find the irred l sums. f(a, b,	obtain undant (c, d) =	7	CO2	L3
2	a	Two motors M2 motor M2 is to run whenever s sensor combina three sensors a truth table and v	2 and M1 are run any time sensors S2 of ations where are off and th write the Boole	controlled by all three senser S1 but not I M1 is on, M2 en both moto ean output eq	y three sen sors are on. both are on 2 is to be o rs must ren uation.	sors S3, S2, The other mo and S3 is of ff except whe nain off. Cons	S1. One otor is to f. For all n all the truct the	7	C02	L3

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34	WGALORE	Title: Course Plan			Page: 37 / 40			
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	b	Implement the b) $f(a, b, c, d)$	multiple functions: a) $f(a, b, c, d) = \sum m(0,4,8,10,14,15)$ . = $\sum m(3,7,9,13)$ , Using two 3 to 8 decoders.	6	C03	L4		
	С	Implement the	following Boolean function with 8:1 multiplexer $f(a, b, c, d) = \sum m(0,2,6,10,11,12,13) + \sum d(3,8,14)$	7	CO4	L4		
3	a	Explain the fo a.Switch debo its eliminatior	llowing: ouncing and its elimination.b.Race around problem and n	8	CO5	L2		
	b	Derive the cha	aracteristics equations of SR and JK Flip Flops.	6	CO6	L3		
	С	Derive the cha	aracteristics equations of D and T Flip Flops.	6	CO6	L3		
4	а	Explain Switch	n debouncing and its elimination.	5	CO5	L2		
	b	Analyze the s	ynchronous sequential circuit shown in the figure below.	8	CO8	L4		
	С	Explain Mealy	and Moore Model with block diagram	7	CO8	L2		
5	а	Compare VH	DL and Verilog	5	CO9	L2		
	b	Write a switcl nmos and pm	h level description in VHDL for the inverter circuit with os.	7	CO9	L2		
	С	Given A = 10 XNOR B ii) Shift B tw concatenation	00 and $B = 0011$ , perform the following operations: i) A ro position left logical iii) Reduction NAND iv) Verilog $\{A,B\}$ v) Verilog modules A%B.	8	CO9	L3		
			OR					
	a	Explicate the	structure of verilog module.	6	C09	L2		
	b	Describe scala	ar data type used in VHDL.	7	C10	L2		
	С	Write behavio verilog.	oral description of the full adder circuit using VHDL and	7	CO10	L2		

## 2. SEE Important Questions

Course:		Digital System DEsign					Month	Month / Year Dec /2018			
Crs Code:		17EE35	Sem:	3	Marks:	100	Time:	180			
								minute		es	
	Note	te Answer all FIVE full questions. All questions carry equal marks.				-	-				
Мо	Qno.	Important Qu	estion					Mark	СО	Year	
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		Doc Code: SKIT.Ph5b1.F02			Date:03-08-201	
ANGALON		Title:	Course Plan	Page:	38 / 4	0
Copyrig	ht ©2017	CAAS. All rights reserve	ved. Dational logic Circuit with the belo of block diagram	г	C01	1.2
1	ו ר		5	C01		
	Ζ	explanation	nowing terms along with appropriate examples for better	8	COT	LZ
		a.Literal b.Mir f.Normal SOP	nterm c.Maxterm d.Canonical SOP e.Canonical POS			
			a. $f(X,Y,Z) = \sum_{i=1}^{N} (0,2,4,6) + dc(7)$			
	3	Express the for write maxterm	ollowing SOP expressions into minterm list form and hence list	6	C01	L3
		a. f(a,b,c,d b. f(a,b,c,d	$ \begin{aligned} f(t) &= (a'b'c + ab'd + abcd + a'b'cd + abc'd) \\ f(t) &= (a'b'c + ab'd + abcd + a'b'cd + abc'd) \end{aligned} $			
	4	Find all the Prime	e Implicants of the function $f(a, b, c, d) = \pi M(0,2,3,4,5,12,13) +$	8	C02	L2
		$\pi d(8,10)$ using (	Quine Mc-Cluskey method.			
	5	Two motors M motor M2 is to run whenever sensor combin three sensors truth table and	7	C02	L3	
2	1	Design a Co binary no. and Output: A=B,	mbinational Circuit that accepts two unsigned 2-bit d provides 3 outputs. Inputs: A=A1A0 and B= B1B0 A>B, A <b.< td=""><td>5</td><td>CO3</td><td>L4</td></b.<>	5	CO3	L4
	2	Implement the b) $f(a, b, c, d)$	multiple functions: a) $f(a, b, c, d) = \sum m(0,4,8,10,14,15)$ . = $\sum m(3,7,9,13)$ . Using two 3 to 8 decoders.	5	CO3	L4
	3	Implement the	following Boolean function with 8:1 multiplexer $f(a, b, c, d) = \sum m(0,2,6,10,11,12,13) + \sum d(3,8,14)$	5	CO4	L4
	4	Design and in	nplement a 4-bit look ahead carry adder.	7	CO3	L4
	5	Design a co Configure the	mparator to check if two n-bit numbers are equal. ese using cascaded stages of 1-bit comparators.	5	CO4	L4
-	1	Evolation alson C	llouing	0	COF	12
3	1	Explain the fo a.Switch debo its eliminatior	buowing: buncing and its elimination. b.Race around problem and n	8	CO2	L2
	2	Explain basic	bistable element	5	CO5	L2
	3	What is mean triggering me	t by triggering of flip-flops? Name the different thods.	5	CO5	L2
	4	Derive the cha	aracteristics equations of SR and JK Flip Flops.	6	CO6	L3
	5	Derive the cha	aracteristics equations of D and T Flip Flops.	6	CO6	L3

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A POTOK	Doc Code:	SKIT.Ph5b1.F02	Date:03-08-2018					
SANGALORE	Title:	Course Plan	Page: 39 / 40					
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4	1	Understand the Mealy & Moore models using their Block diagrams.	8	C07	L2
	2	Analyze the synchronous sequential circuit shown in the figure below. A = A = A = B = A = A = A = A = A = A =	8	CO8	L4
	3	Construct the state table for the following state diagram.	10	CO7	L4
	4	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with JK flip-flop.	8	CO8	L4
	5	For the logic diagram given in figure, a)Derive the excitation and output equations. b)Write the next state equations c)Construct a transition table and d)Draw the state diagram. $x + f_{F_1} + f_{F_2} + f_{F_1} + f_{F_2} + f$	8	CO8	L4

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		Doc Code:						
10	ANGALORE	Title:	Course Plan	Page	: 40 / 4	łO		
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5	1	Explicate the	structure of verilog module.	5	C09	L2		
		-						
	2	Describe scal	ar data type used in VHDL.	5	C10	L2		
	3	Discuss logic	al and arithmetic operators used in VHDL.	6	CO5	L2		
	4	Elaborate any	v two data types used in verilog.	4	CO5	L2		
	5	Write behavio	oral description of the full adder circuit using VHDL and	4	CO5	L2		
		verilog.						
	6	Write a switc	h level description in VHDL for the inverter circuit with	6	CO5	L2		
		nmos and pm	OS.					